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16 INPUT/1 OUTPUT SWITCHING MATRICES.(U)
APR 77 P J HAGON, D PENUNURI F19628-75-C-0175
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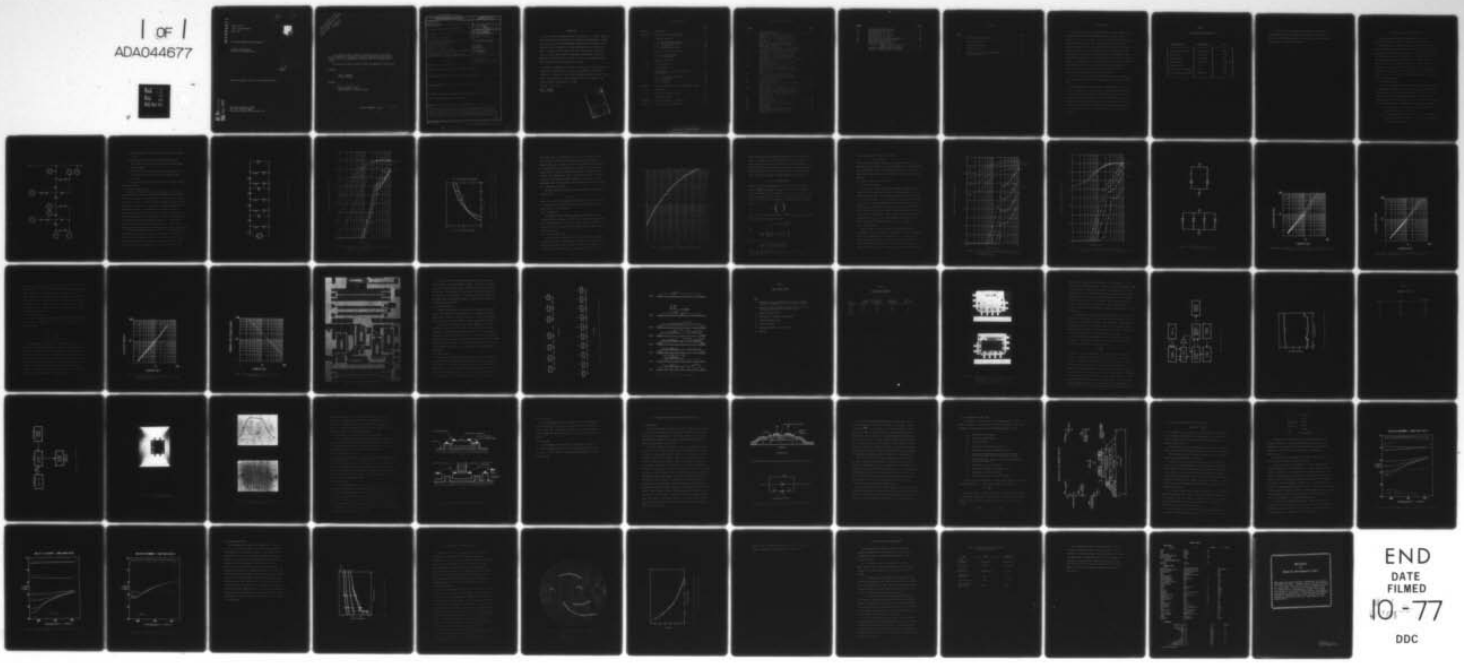

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Final Technical Report
April 1977

16 INPUT/1 OUTPUT SWITCHING MATRICES

Rockwell International
Electronics Research Center

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This technical report has been reviewed and approved for publication.

APPROVED:

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FOR THE COMMANDER:

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The design, fabrication and performance of a 16 input/1 output UHF switch matrix is described in this report. Each switch consists of silicon-on-sapphire PIN diodes, operates in the frequency range 950-1220 MHz, provides 60 dB on-off ratio, and reduces the DC power consumed relative to a previous device (Report AFGL-TR-76-0016) by using miniature integrated inductors.

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EVALUATION

1. This is the Final Technical Report on the contract. It covers research done on switching matrices during the full period of performance. Progress was made in the on-off ratio and power consumption of the switches, and in demonstrating the feasibility of integrating amplifiers into the switch chips. A study was made of the possibility of fabricating a resistive gate switch which would greatly reduce power requirements, as power is only used in swtiching from on to off or off to on, as opposed to the PIN diodes switches which require power at all times.

2. Frequency synthesizers are finding increasing use in miliary and other systems due to the efficiency in making a large number of frequencies available, all locked to a single stable reference frequency source. Fast, compact switching matrices such as these will allow more compact, fast hopping frequency synthesizers to be made.

Alan J Budreau

ALAN J. BUDREAU
Project Engineer

C O N T E N T S

ILLUSTRATIONS

TABLES

1.0 INTRODUCTION

The major objective of this program phase has been to improve the compact microwave frequency, 16-input/1-output, switching arrays developed in the previous phase. The device characteristics and improvements are summarized in Table 1. As with the previous device, the technology selected for the improved device switch consists of a combination of vertical junction PIN diodes on a silicon-on-sapphire (SOS) substrate. As seen in Table 1, the major points of improvement consist of increasing the ON/OFF ratio by 15 dB and reducing the DC power dissipation. The improved on-off ratio was achieved by increasing the number of PIN diodes from three to six. The second goal was achieved by replacing the silicon resistors used in the previous device for RF isolation and ground returns with planar inductors.

In Section 2.0, the design and experimental results of the improved device are presented together with installation and operation recommendations.

Also investigated during this phase of the contract is the feasibility of a Resistive Gate Switch (RGS). The advantage of this device is that no DC power is required to maintain the switch in either the ON or OFF states. The only power required is that necessary to charge or discharge the MOS gate capacitance during a state transition (ON / OFF or OFF / ON). An RGS device was included in the switch array mask set and in Section 3.0, the design and experimental results of this study are presented.

TABLE 1

SWITCH ARRAY CHARACTERISTICS

Characteristic	Previous Device	Goal
Frequency of Operation	0.95-1.22 GHz	Same
On-Off Ratio	50 dB Min.	65 dB
Switching Time	1 μsec Max.	Same
DC Dissipation	50 mW Max.	40 mW Max.
Insertion Gain	----	5 dB
Insertion Loss Uniformity	1 dB	Same
Power Handling Capability	10 mW Min.	Same

A third task of this contract is to study the feasibility of incorporating an amplifying stage with each switch in the array. To this end an SOS/MOS FET device was also included in the switch array mask set and is discussed in Section 4.0.

2.0 DESIGN OF THE 16X1 SWITCH ARRAY

The final switch design is an extension of the previous 16 input/1 output type of switch. The major revisions consisted of (1) incorporating square planar inductors to be used as RF chokes which replaced the resistors in the previous switch and (2) increasing the number of PIN diodes to six in order to improve the on-off ratio. The final switch circuit is seen in Figure 1. R_1 through R_5 are the residual resistances of each inductor. The switch circuit is seen to consist of two 3-diode Tee sections in series. Each Tee section has a separate ground and bias pad. It is felt that this is the only means by which the 65 dB on/off ratio can be achieved in so compact a circuit. The design of the switch parameters is discussed in the following sections.

2.1 Integrated Inductors

The use of integrated inductors to replace the bias port isolation and ground return resistors of the previous design is the principal technique by which the DC power requirements of the switch array can be reduced. Then only the residual metallization resistance of the inductor turns and the diodes remain to dissipate DC power. The design of the required inductor is determined by the following constraints:

(1) The physical size of the inductor must be minimized if a compact switch array is to result.

(2) The inductance must be large enough to give an acceptable value and uniformity of insertion loss in the frequency band of interest, 950-1220 MHz.

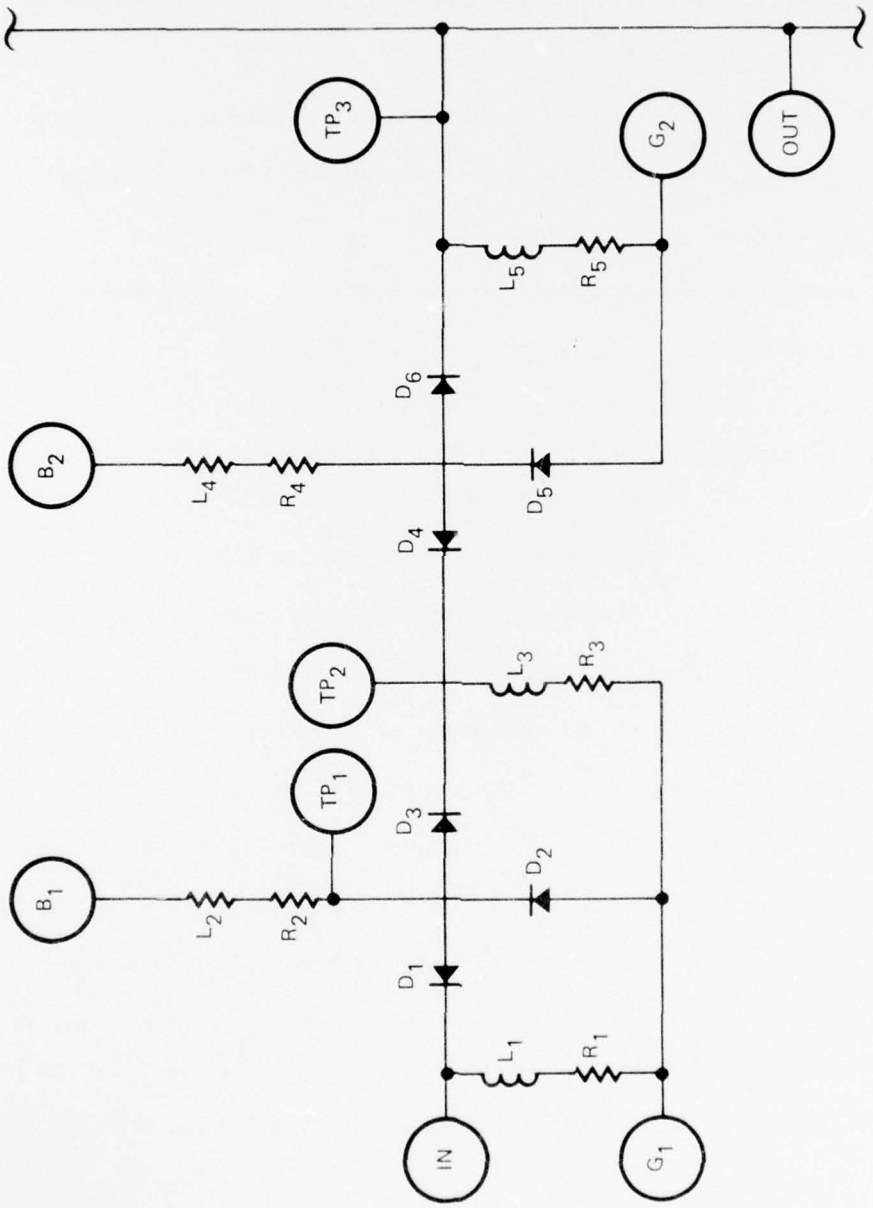


Figure 1. Six Diode Switch Circuit

(3) The inductance must not increase the switching time beyond 1 μsec.

(4) The inductor metallization width and thickness must be sufficiently large in order to handle the expected biasing current density.

(5) The chokes must not couple via mutual inductance or stray capacitance within a given switch and between adjacent switches.

In the following sections, the tradeoffs among the above requirements is discussed.

2.1.1 Minimum Inductance Value

In order to determine the range of inductance values which are compatible with the above insertion loss requirements, the effective RF circuit in Figure 2 was analyzed under the conditions that all six diodes are identical, so that the forward resistance R_d and the depletion layer capacitance C_d is the same for all diodes, and that all five inductors are identical. Measurements of previously fabricated inductors indicate that a Q in the range of 5 to 10 is achievable at 1 GHz with only minor processing changes. Therefore, for convenience, the calculations below assume inductors with $Q = 2\pi$. The effect of varying the inductance from 5 to 25 nH in steps of 5 nH is seen in Figure 3, which shows the "on" state insertion loss and the on-off ratio as a function of frequency from 0.1 to 10 GHz. The calculation was performed over two decades of frequency for diagnostic purposes. The data of Figure 3 is reduced in Figure 4 to show directly the effect of the choke inductance or resistance on the insertion loss at 1.2 GHz and the difference in insertion loss at 0.9 GHz and 1.2 GHz. The

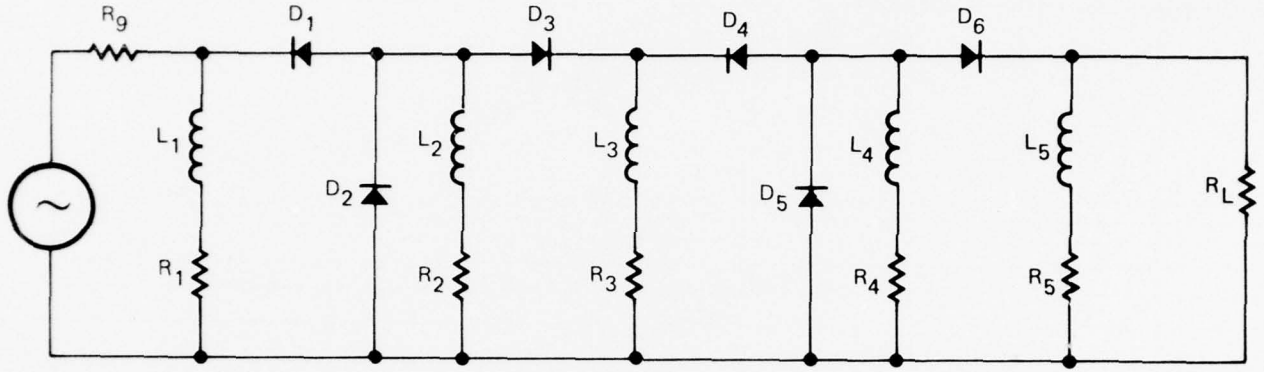


Figure 2. Effective RF Circuit

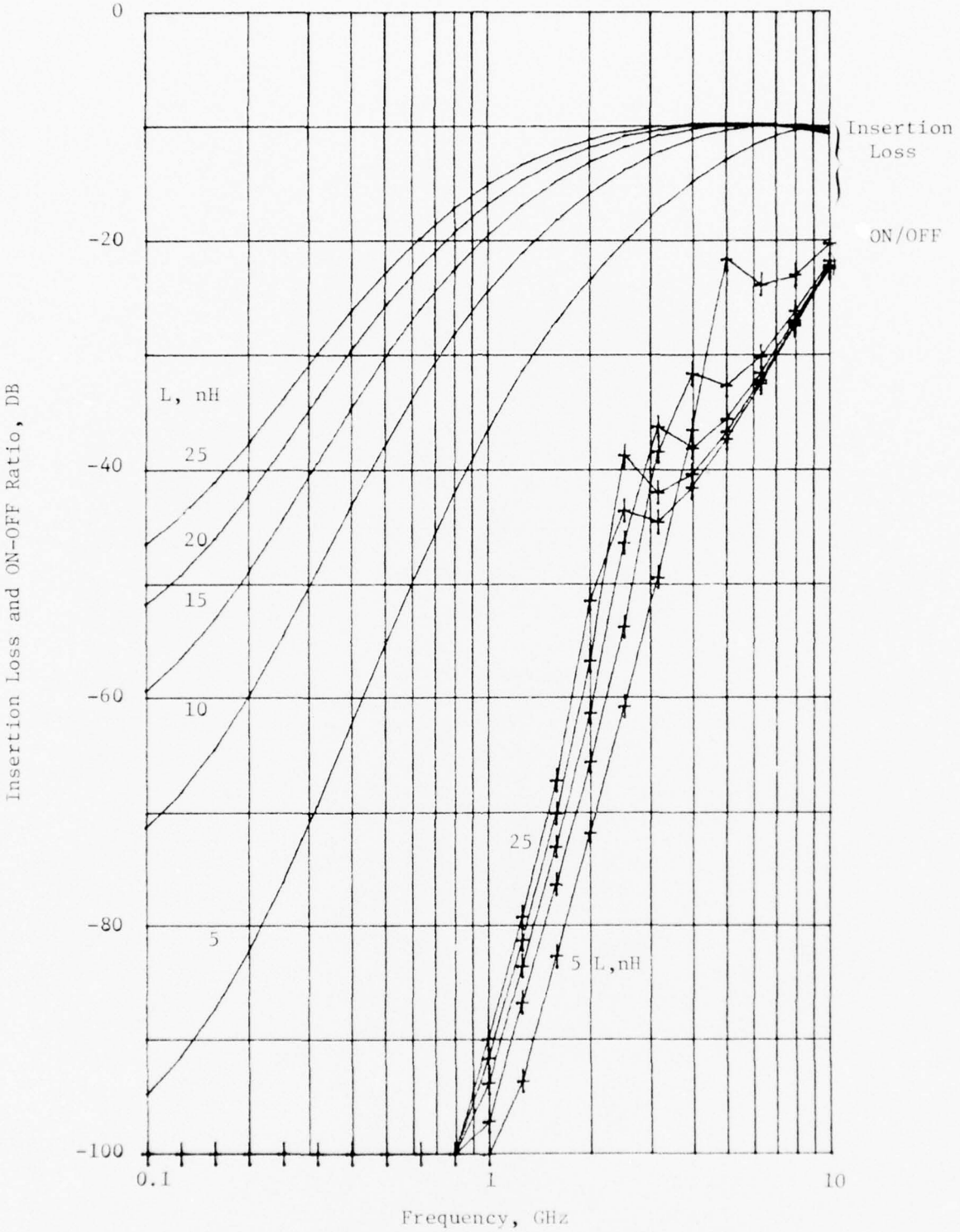


Figure 3. Insertion Loss and ON-OFF Ratio Versus Frequency. $R_d = 50\Omega$, $C_d = 0.1$ pF, $R_g = R_L = 50\Omega$. The Parameter is Choke Inductance

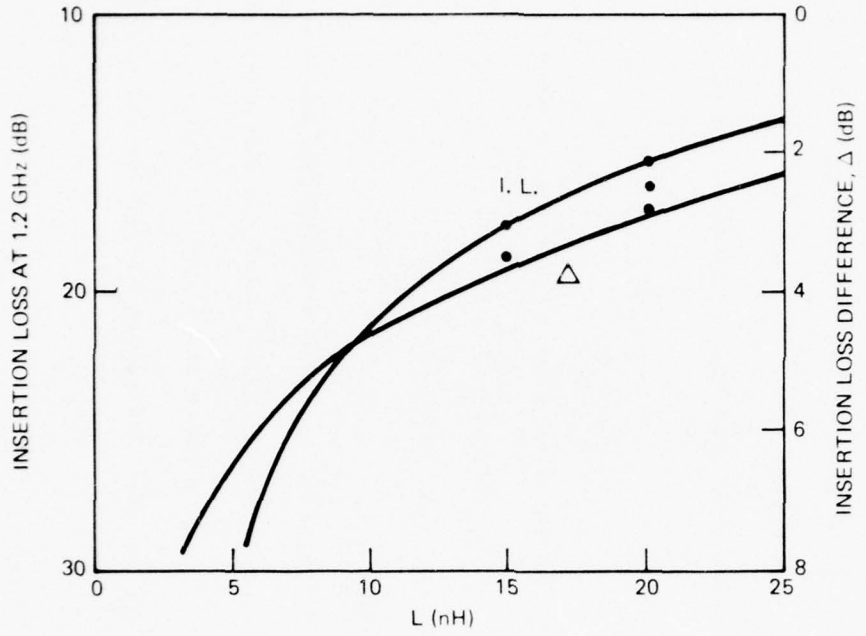


Figure 4. Insertion Loss at 1 GHz and Insertion Loss Difference (900 MHz Versus 1200 MHz), Versus Choke Inductance

figure shows that if the insertion loss is to be less than 20 dB and vary less than 3 dB across the band, then the inductance must be greater than 13 nH. In Figure 5 is seen the inductance and resistance of a typical square planar inductor as a function of the side of the square in mils. The most compact geometry which is judged practical consists of an inductor with turns 5 μm wide and spaced 10 μm center-to-center. This geometry has been assumed in the calculation. The graph shows that a 20 nH inductor will occupy an area of 144 square mils.

2.1.2 Switching Time Effect

The bias current rise time due to the presence of the inductors is estimated from

$$\tau = L/R$$

where L and R are the inductance and resistance of the RF choke. If L = 20 nH and R = 20 Ω, then the rise time of the inductor is 1 nsec, well within the 1 μsec maximum.

2.1.3 DC Capability

Measurements indicate that thin aluminum stripes will survive current densities in excess of $2X10^{10}$ A/m^2. A current of 5 mA flowing in an inductor stripe 1 μm thick and 5 μm wide implies a current density of 10^9 A/m^2 so that the switch should survive current pulses in excess of 10 mA.

2.1.4 Inductor Cross-talk

The only potential problem at this time is inductor-to-inductor cross-talk via mutual inductance and capacitance. A mask was fabricated which contains several inductor test patterns arranged with typical switch-to-switch spacing. Thus, the 1 GHz behavior of the

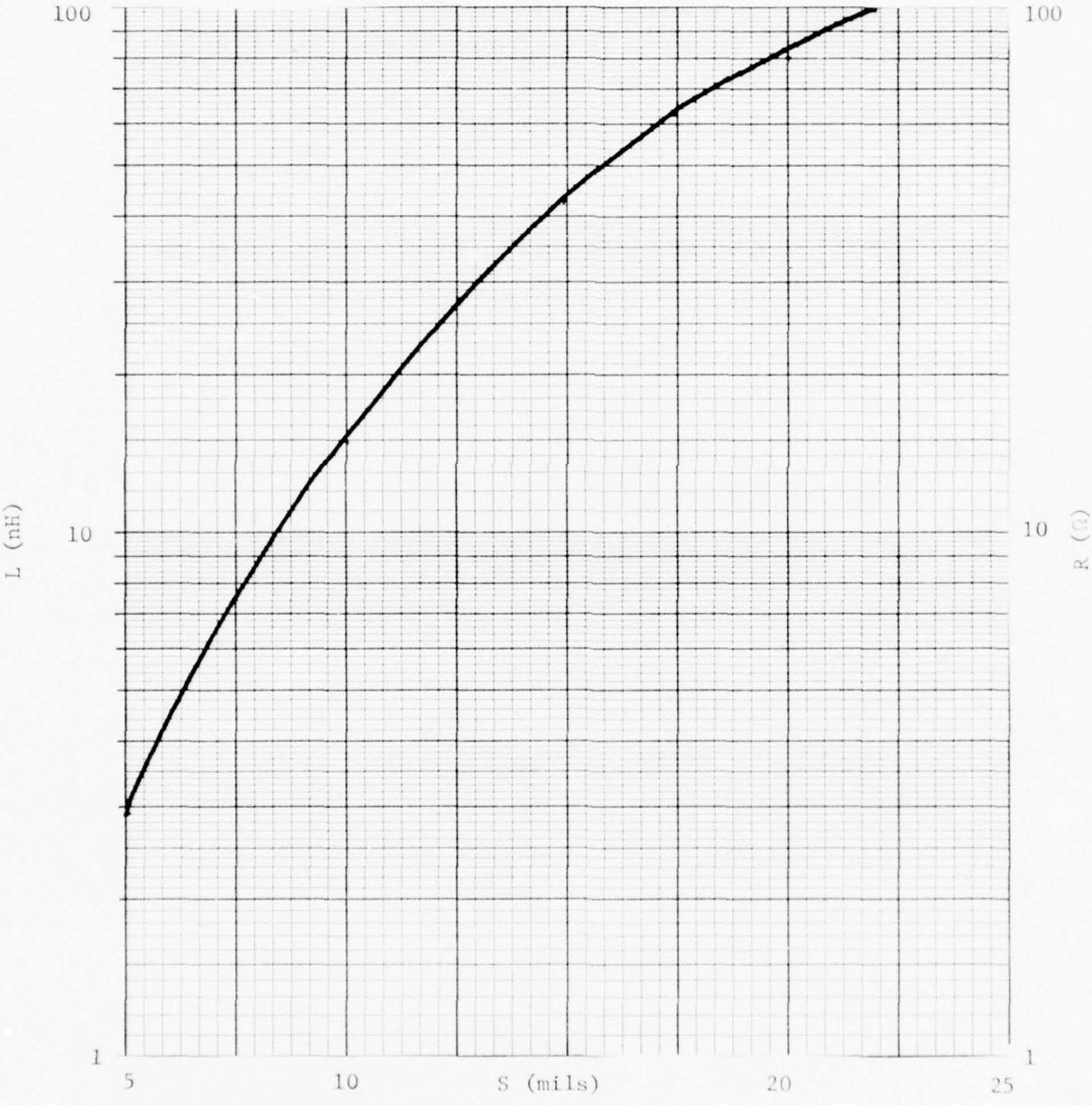


Figure 5. Inductance and Resistance of a Square Planar Inductor Versus Side Length S of the Square

square planar inductor was evaluated independently on a sapphire substrate. Concurrently, an analysis was undertaken to estimate the mutual inductance and, hence, cross-talk. The mutual inductance between two similar square planar inductors was approximated by using the empirical formula* for two coplanar circular current filaments, each of which have a radius R, and are separated by a distance ℓ,

$$M = 10^{-3}\, R\, \frac{\pi^2}{8} \left(\frac{2R}{\ell}\right)^3 D\left(\frac{2R}{\ell}\right)$$

where M is the mutual inductance in μH, R and ℓ are in cm and the function $D\left(\frac{2R}{\ell}\right)$ is tabulated by Grover. In the case of switch-to-switch cross-talk, $\frac{2R}{\ell} = 0.2$ and $D\left(\frac{2R}{\ell}\right) = 1.02$. Then M = 0.3 pH. Since the self inductance of such coils is L = 20 nH so that $\frac{M}{L} = 1.5 \times 10^{-5}$ If the pair of inductors is modeled as a two-port, then the impedance matrix is

$$Z = j\omega \begin{pmatrix} L & -M \\ -M & L \end{pmatrix}$$

where ω is the radian frequency and $j = \sqrt{-1}$. Therefore, the insertion loss from a generator R_g to a load R_L is

$$I.L. = 10\ \mathrm{Log}_{10}\ \frac{4R_g |G|^2}{R_L}$$

where

$$|G|^2 = \left\{ \left(\frac{L}{M}\right)^2 + \omega^2\, \frac{(L^2 - M^2)^2}{M^2\, R_L^2} \right\}^{-1}$$

and if $M \ll L$ then

$$|G|^2 = \left(\frac{M}{L}\right)^2 \left\{ 1 + \left(\frac{L\omega}{R_L}\right)^2 \right\}^{-1}$$

---

* F. W. Grover, Inductance Calculations, D. Van Nostrand Company, Inc., New York, 1946.

In the case of switch-to-switch cross-talk

$$I.L. = -100 \text{ dB}.$$

Since the input and output inductors, L_1 and L_5 (see Figure 1), are grounded, it was assumed that their mutual capacitance is insignificant. The test inductors yielded similar experimental results in that no signals were present down to the -90 dB level, the limit of the network analyzer.

2.2 Circuit Analysis of the Switch

2.2.1 RF Circuit Analysis

The effective circuit in Figure 2 was used to evaluate the performance of the 6-diode switch versus the diode parameters R_d and C_d. Figure 6 shows the "on" state insertion loss and the on-off ratio for R_d = 10, 20, 40 and 80 Ω. It is seen that a 65 dB on-off ratio requires that $R_d \leq 100$ Ω. The ion-implanted PIN diodes fabricated previously exhibited R_d in range 10-20 Ω so that the on-off ratio should exceed 65 dB. Figure 7 shows the "on" state insertion loss and on-off ratio for C_d = 0.05, 0.10, 0.15 and 0.20 pF. Again, the 65 dB on-off requirement implies that $C_d \leq 0.2$ pF. Measurements indicate that for the diodes to be used within this switch $0.05 \text{ pF} \leq C_d \leq 0.08$ pF.

2.2.2 DC Performance

The DC circuit is seen in Figure 8. Assuming the diode I-V characteristic which was measured on previously fabricated ion-implanted diodes, the resulting DC power dissipation versus current for an RF choke resistance R_c = 0, 25, 50, 75, 100 Ω is seen in Figure 9. If the biasing current can be kept at or below 20 mA the dissipated power will be below 40 mW. The power curves are relatively insensitive

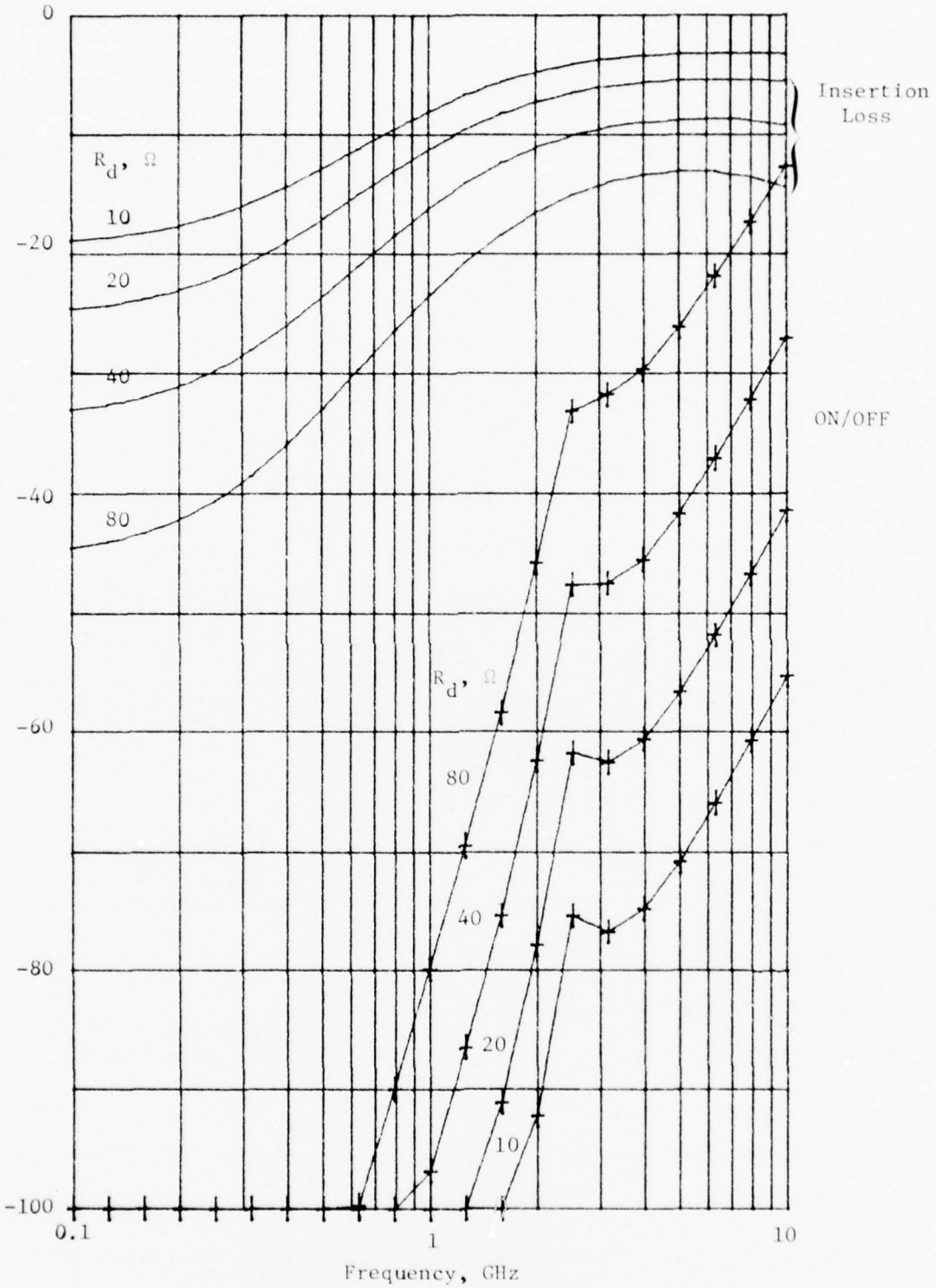


Figure 6. Insertion Loss and ON-OFF Ratio Versus Frequency
C_d = 0.1 pF, R_g = R_L = 50Ω, L = 20nH, R_c = 50Ω.
The Parameter is R_d

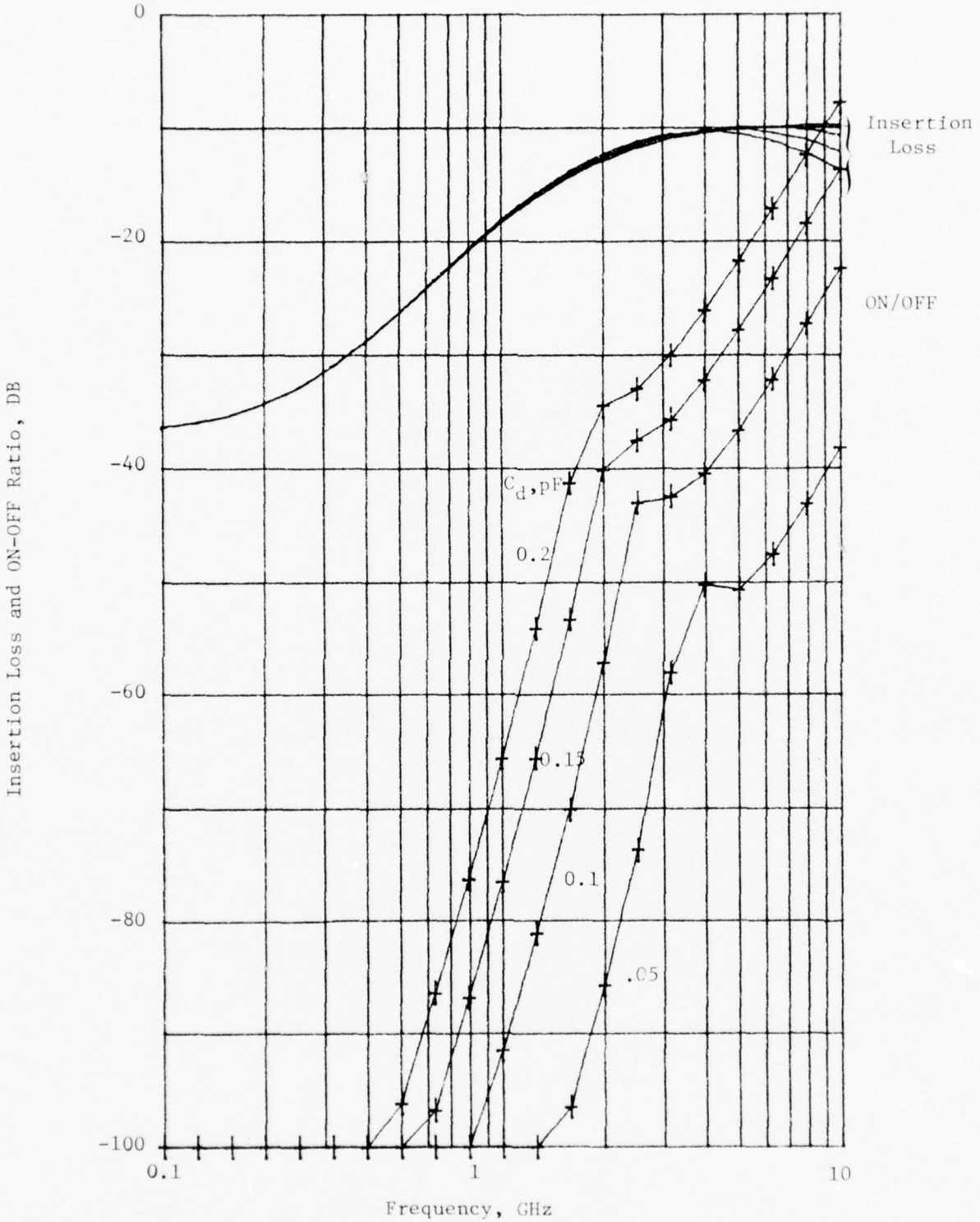
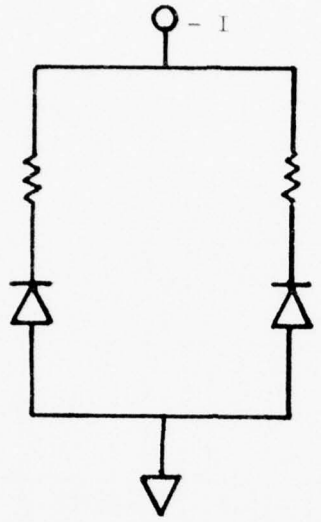


Figure 7. Insertion Loss and ON-OFF Ratio Versus Frequency. $R_c = R_d = R_g = R_L = 50\Omega$, L = 20nH. The Parameter is CD.



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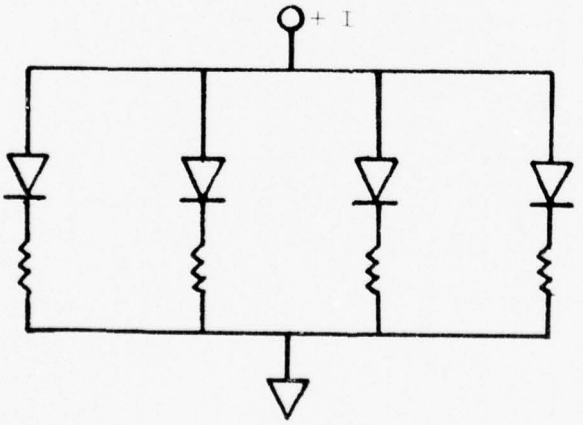


(b)

Figure 8. (a) "ON" Effective DC Circuit.
(b) "OFF" Effective DC Circuit.

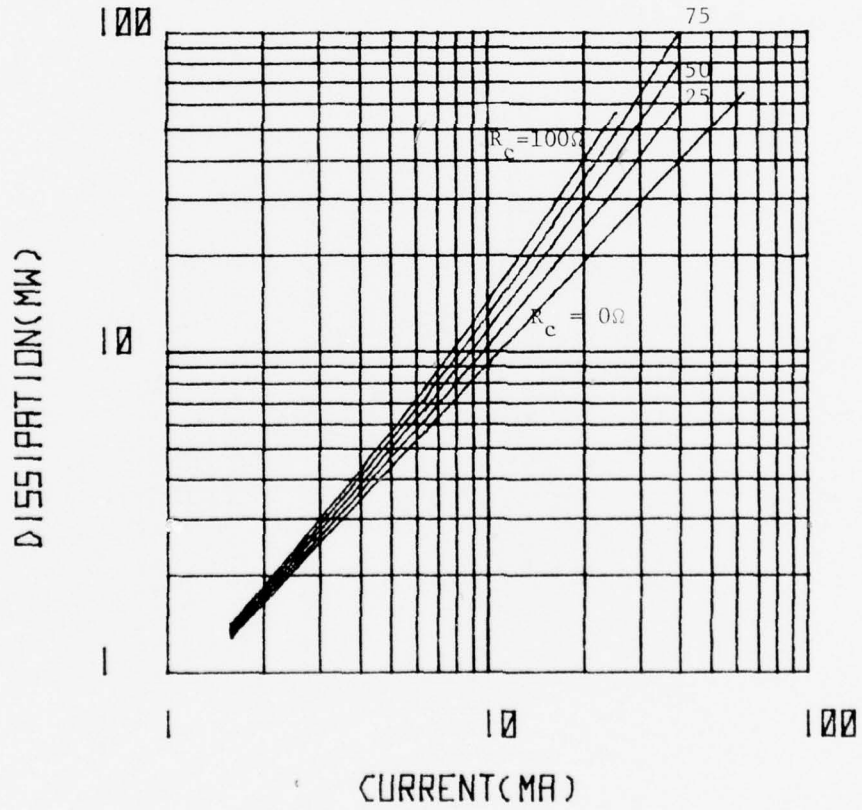


Figure 9.(a) Dissipated Power Vs. Bias Current. Diode Width is 5 mils. The Parameter is Choke Resistance, R_c. (a) "ON" State.

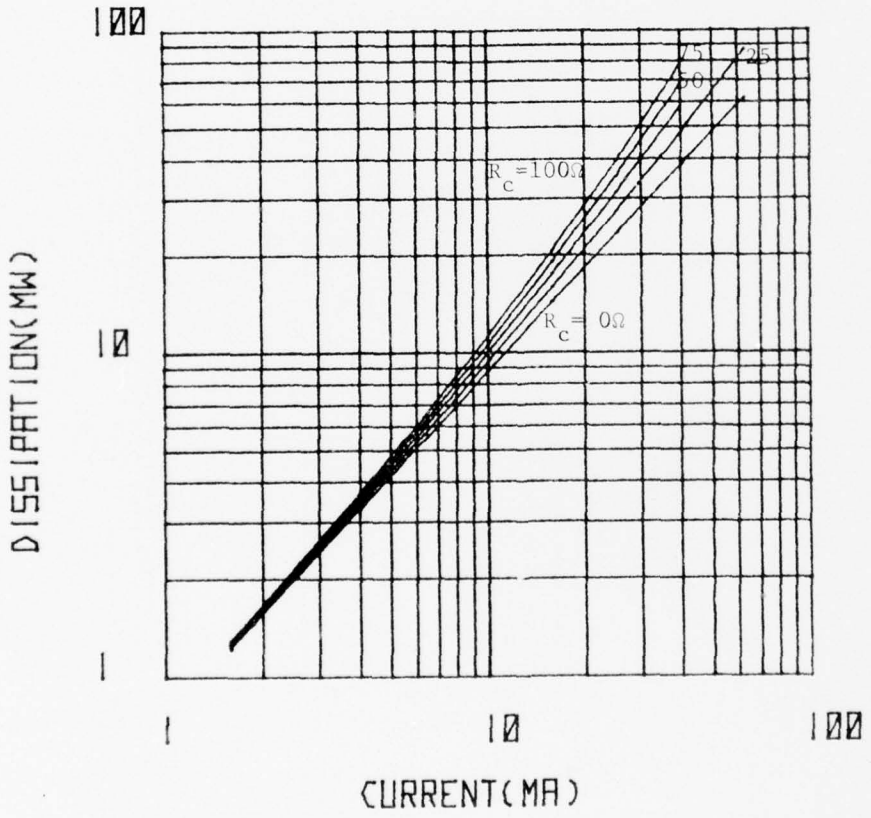


Figure 9.(b) Dissipated Power Vs. Bias Current, Diode Width is 5 mils. The Parameter is Choke Resistance, R_c. (b) "OFF" State.

to the coil resistance in the range considered (0 to 100 Ω). Since the diode width L is the only physical dimension which can be adjusted easily the variation of dissipated power for several values of L is seen in Figure 10. In this case the RF choke resistance is held constant at 50 Ω and L = 5, 10, 15, 20 mils. Once again the power curves are insensitive to the diode width. In Figure 11 is seen the dynamic resistance R_d of the diodes which results corresponding to the above dissipation calculations.

2.3 Layout of Switch Cell

In order to simplify the layout, all six diodes were chosen to be 10 mils wide. The target values for the various circuit elements are summarized below:

$$R_d \quad \leq 50\ \Omega$$

$$C_d \quad \leq 0.1\ \text{pF}$$

$$L \quad \geq 20\ \text{nH}$$

$$R_c \quad \leq 50\ \Omega$$

A photograph of the circuit for a single switch is seen in Figure 12. The DC blocking capacitors present in the previous switch design are not required here. The reason is that the DC voltage expected across inductor L_1 and, hence, across the input terminals is only a few tenths of a volt. As noted above, each switch in the array has two separate DC bias bonding pads and two separate grounds. The separation is necessary to avoid the "floating ground" situation caused by the small but non-zero inductance of the ground bond wires (noted in Scientific Report No. 1, AFGL-TR-76-0016).

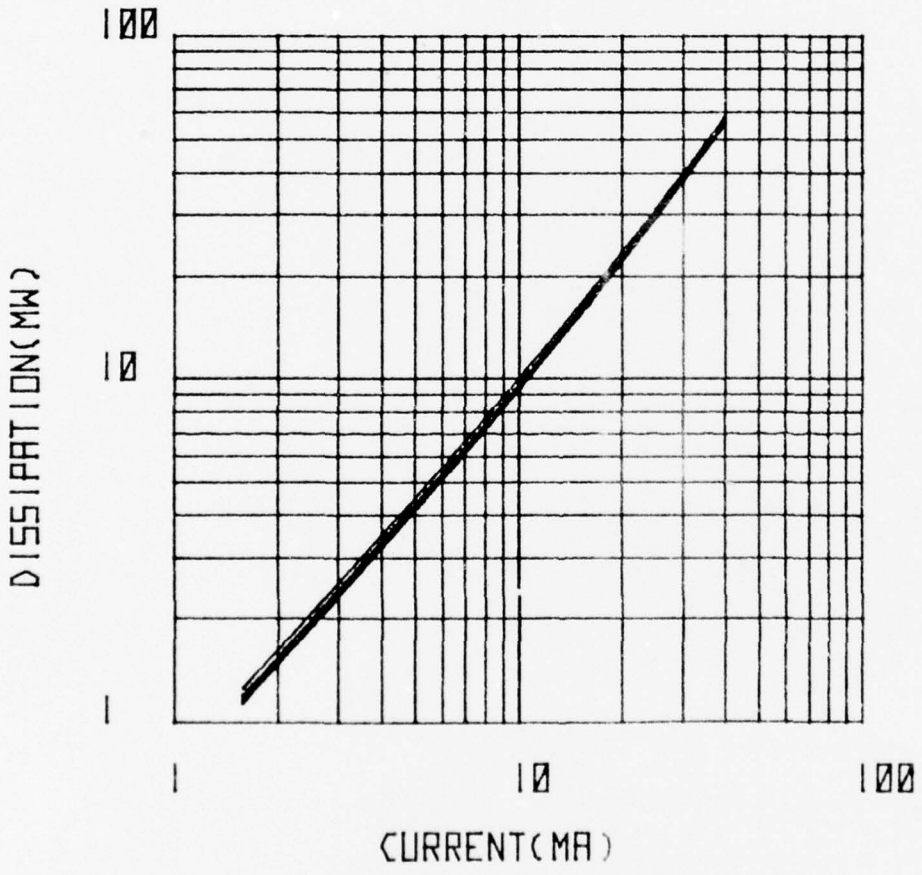


Figure 10. Dissipated Power Versus Bias Current. $R_c = 20\Omega$. The Parameter is Diode Width Dynamic Resistance Versus Bias Current.

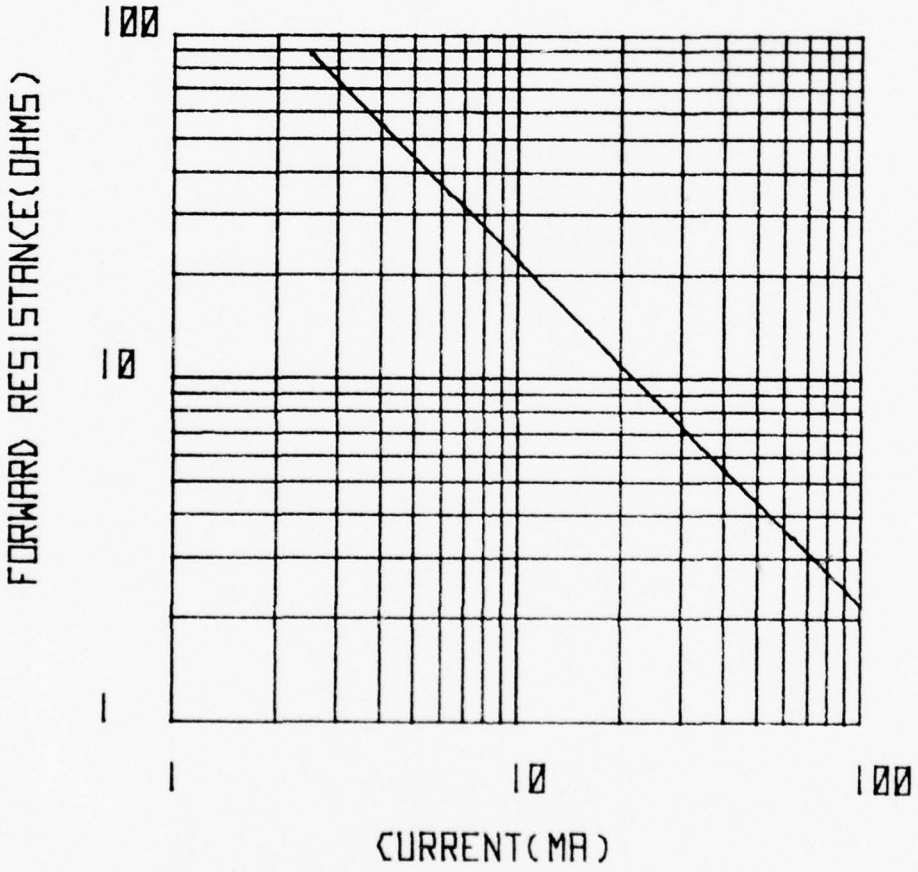


Figure 11. Dynamic Resistance Versus Bias Current. $I_o = 3X10^{-10}A$ and M = 2.2

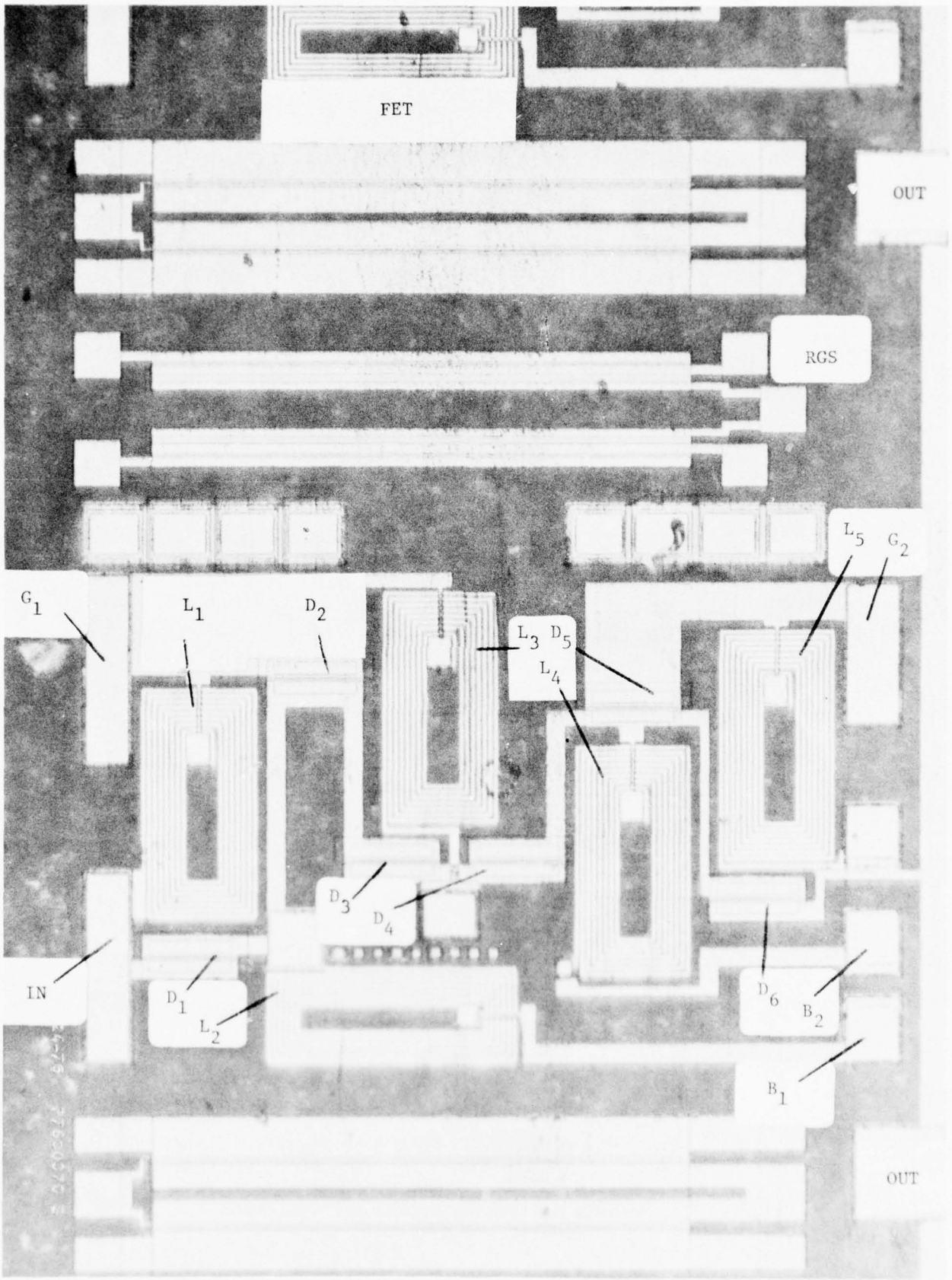


Figure 12. Layout of the Switch

Initially, the switch array was arranged as a 17X1 with 55 mil switch spacing. At the Government's request, the layout was modified to provide for two separate arrays: A 9X1 array with 122 mil switch spacing and a 7X1 array with five spacings of 100 mils and one spacing of 150 mils, as seen in Figure 13. The change doubled the length of the switch array and reduced the number of possible switch arrays per 2" SOS wafers from 20 to 10.

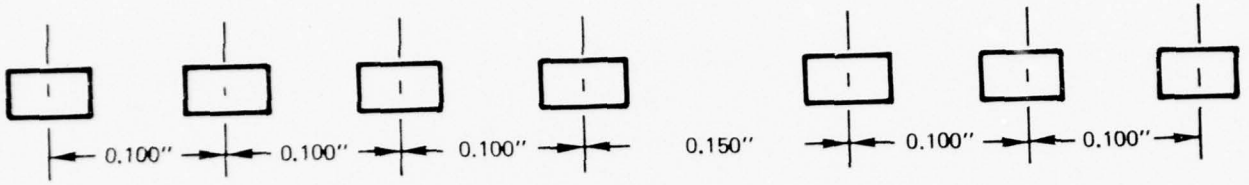
2.4 Device Fabrication

A modified doped oxide process was used to fabricate the switch arrays. The modifications were necessary to accommodate the double-metallization required to achieve low resistance inductor corss-unders. The process steps are seen in Table 2 and are illustrated in Figure 14.

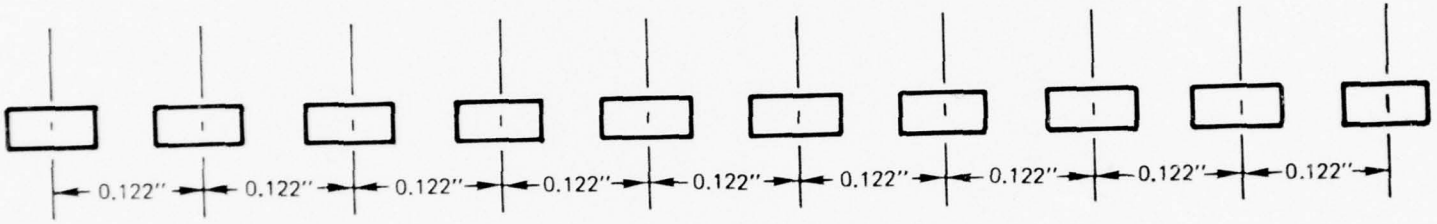
One lot of nine wafers was processed to completion. The wafers originally consisted of a 0.7 μm (100) Si film on a 13 mil, (1102), sapphire. The resistivity was greater than 300 Ω-cm. The implantation schedule for each wafer is seen in Table 3. Data from a test resistor indicated that the I-region resistivity is about 30 Ω-cm which is adequate from good diode performance. After ion implantation, the wafers were processed normally as per Table 2. No problems were encountered during processing.

2.5 Device Results.

Fully functional switch arrays were identified by performing (1) a visual inspection for physical defects in metallization, e.g., shorted or open inductors, etc., and (2) testing the bias port for conduction. An RF test package was constructed which provided 9 dc biasing lines, 9 RF input lines with OSM type coaxial connectors, and 1 RF output line as seen in Figure 15. The package also contains an electromagnetic



7 x 1 ARRAY



9 x 1 ARRAY

Figure 13. Switch Spacings Required for the 9X1 and 7X1 Switch Arrays

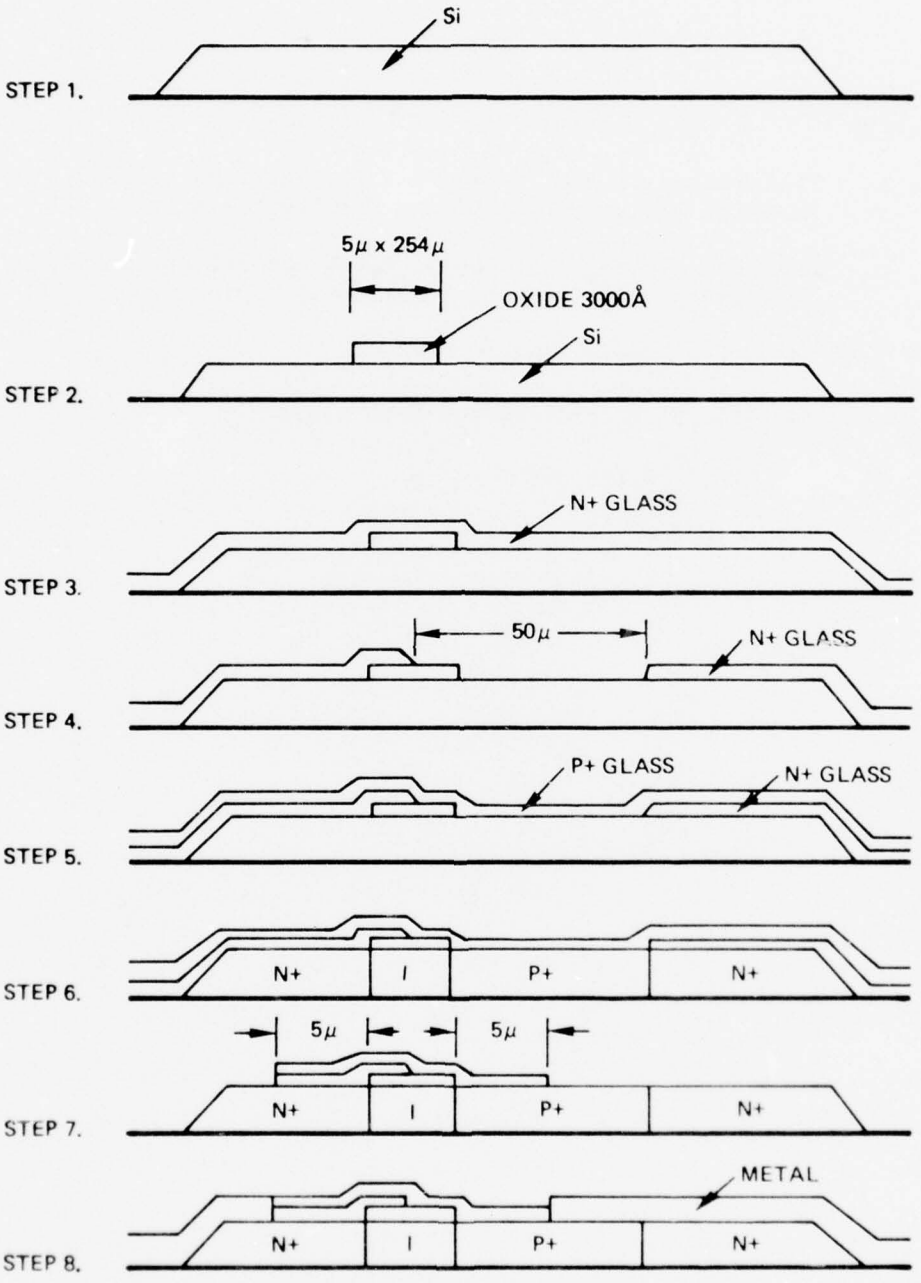


Figure 14. Doped Oxide Process Sequence

TABLE 2

DOPED OXIDE PROCESS

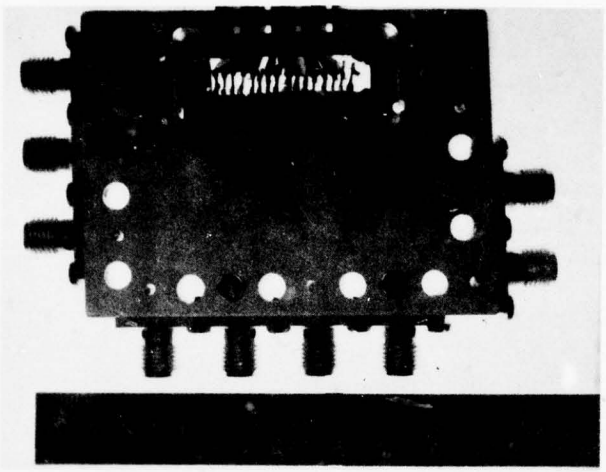
Step

1. Photoresist silicon island and etch silicon islands, removing all unwanted silicon from sapphire substrate.
2. Oxidize silicon, photoresist I-regions and etch oxide, leaving an oxide bar which defines I-region.
3. Deposit N^+-doped glass.
4. Photoresist P^+ pattern and etch glass.
5. Deposit P^+-doped glass.
6. Drive in dopants.
7. Photoresist contacts and etch glass.
8. Metalize.

TABLE 3

IMPLANTATION SCHEDULE

Wafer #	Incident Ion Density X10^{10} cm^{-2} 25 kev	200 kev	400 kev	No. 10^{14} cm^{-3}
1.2.3	1.08	0.9	1.6	4
4,5,6	1.52	1.26	2.24	6
7,8,9	2.1	1.8	3.1	8



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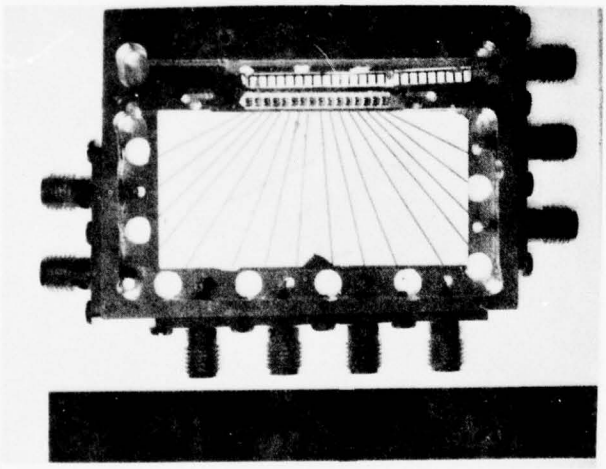


(b)

Figure 15. RF Test Package. (a) Top View Showing Fan-Out Pattern, Switch Array and Output Sumline. (b) Bottom View Showing DC Bias Line Ribbon, DC Feed-throughs, and RF Bypass Chip Capacitors.

shield used to reduce direct feed-through. A block diagram of the RF test set-up is seen in Figure 16. In order to increase the dynamic range of the system, a 20 dB pad was installed in the reference line of the S parameter test set. The network analyzer was calibrated using precision attenuators before each test. At 1 GHz the noise floor of the system (test arm open), was at -75 dB to -80 dB. Thus, in order to measure the -80 dB or less signal for the switch off state, it was necessary to include an amplifier in the test arm following the switch output as seen in Figure 16.

A DC tested switch array from wafer 5 was installed in the RF test package. All connections were made using thermal-compression bonds consisting of 2 mils diameter gold wire. The results for a typical switch are seen in Figure 17 in the frequency range 950 to 1220 MHz. Table 4 summarizes the RF response of the seven switches in the 7 x 1 array. The minimum on-off ratio was 55 dB and the maximum was 60 dB.

The switching time measurement was performed using the set-up seen in Figure 18. In order to transmit a pulse with rise and fall times of T_r, a low pass system with a minimum bandwidth of

$$f_c = \frac{0.35}{T_r}$$

is required. If good pulse fidelity is required then a bandwidth 4 to 5 times f_c is necessary. Since the switches within a 16 x 1 array are expected to switch in 5 to 10 nsec then f_c is 35 to 70 MHz. Therefore, a single switch was installed in the special test package seen in Figure 19. The package provides 50 Ω microstrip lines (gold on alumina) to the RF output and bias ports of the switch. The RF input of the switch is connected directly to the center-pin of the coaxial connector. The Phoenix generator provides a pulse of amplitude, -2 to +3 V so that the switch is turned ON and OFF. The pulse used to bias the switch is seen in Figure 20 for a 70 Ω load, which approximates the input impedance of

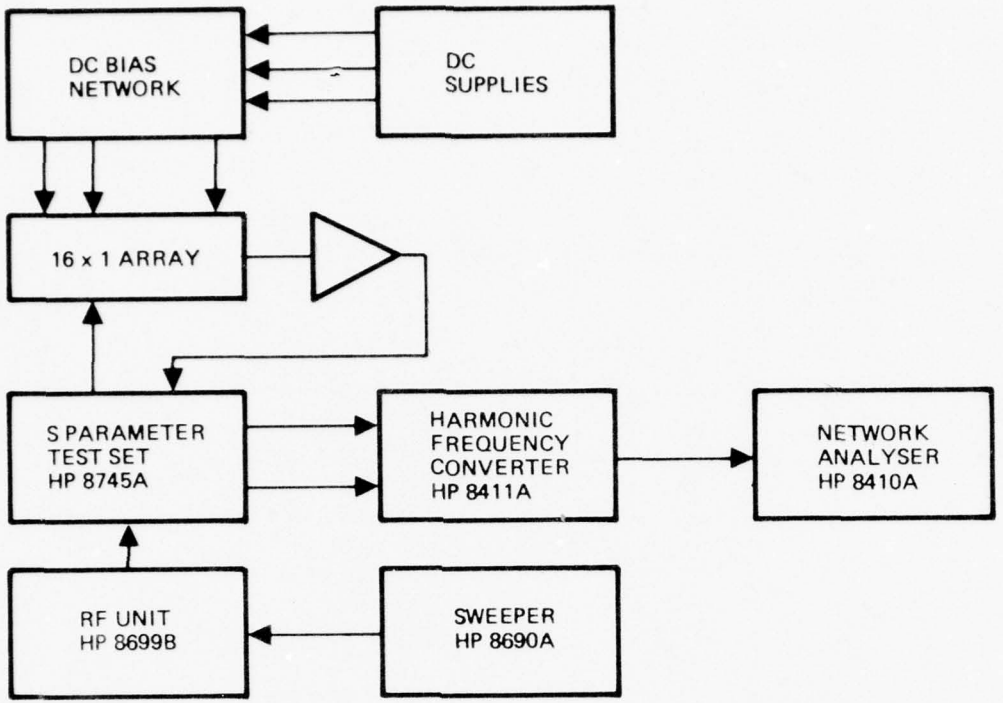


Figure 16. RF Test Set-Up

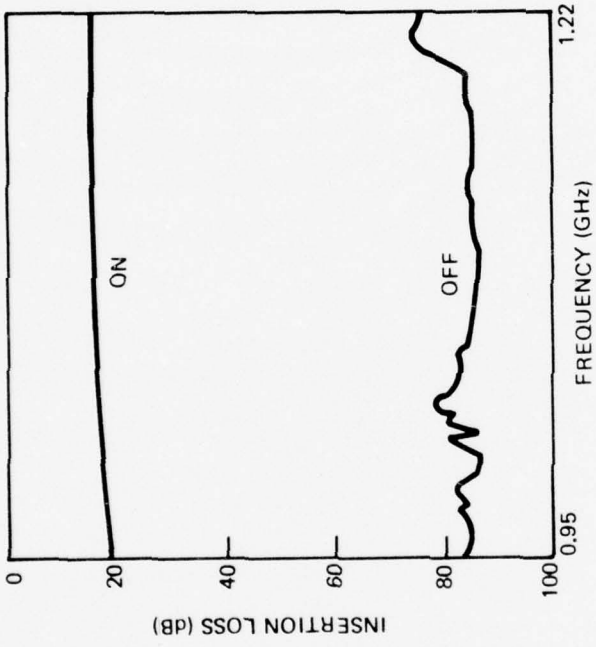


Figure 17. Response of a Typical Switch

TABLE 4

SUMMARY OF RF TEST

Switch	ON, dB	ON-OFF, dB
1	19.5	60
2	19	61
3	19	58
4	18	57.5
5	18	62
6	18	58
7	18.5	60

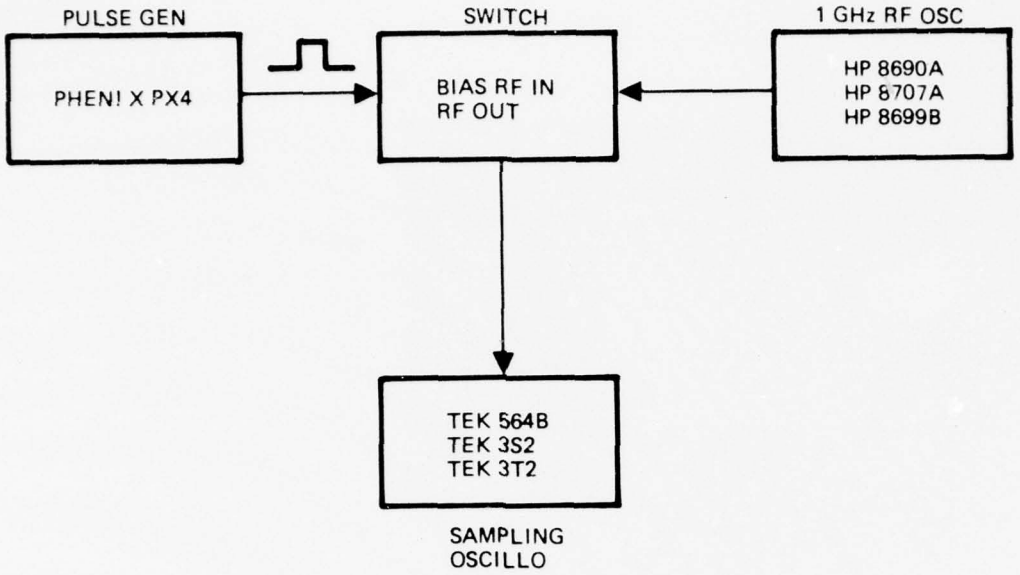


Figure 18. Pulse Test Set-Up

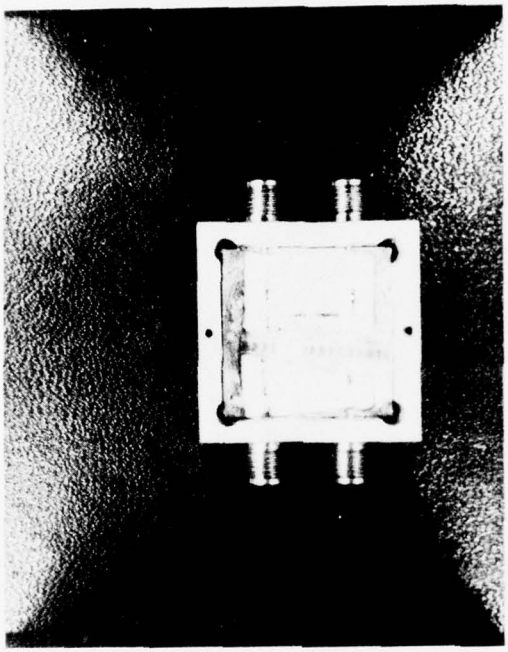
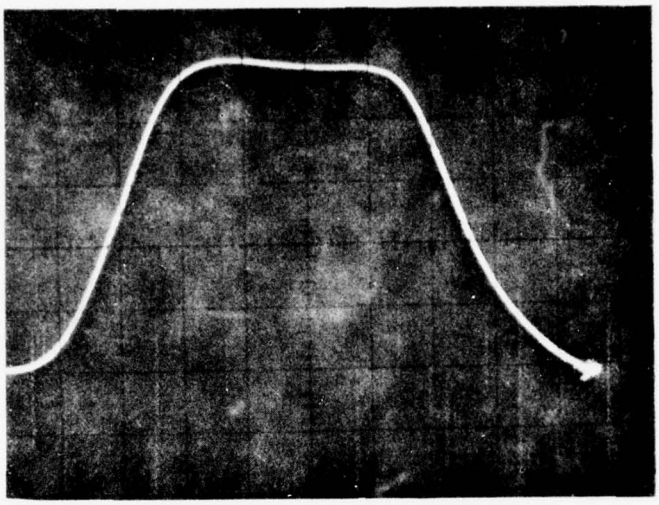
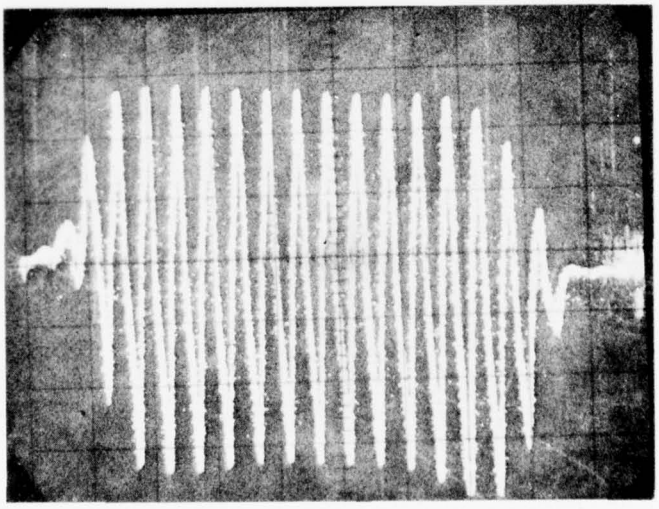


Figure 19. Test Package Used For Switching Speed Measurement



(a)



(b)

Figure 20. Pulse Response. (a) Bias Waveform (b) Switch Response.

the switch biasing port. The switching pulse shows a rise time of 1.6 nsec. The response of the switch to a 1 GHz signal is seen in Figure 20. The switch rise time (10 to 90 percent) is comparable to that of the input pulse indicating that the pulse generator may be the limiting component in the measurement system.

2.6 Recommendations for Device Installation and Operation

It is recommended that the following installation procedures are used in order to fully realize the potential performance characteristics of the devices delivered during this phase of the contract and those devices delivered during a previous phase of the contract.

2.6.1 Installation of the Chip

It is very important that the package be metallic (preferably gold plated) and that the back side (opposite circuit) of the sapphire substrate be in intimate contact with the package. In this manner, most of the stray fields due to the high dielectric constant of the chip substrate, are terminated on the package thus reducing direct feed-through. Such contact is achieved by attaching the chip to the package with a conductive epoxy. (See Figure 21a).

2.6.2 Wire Bonding

The two chip grounds per switch, G_1 and G_2 (Figure 12), should be bonded with large diameter wire, preferably gold ribbon, less than 25 mils long (if possible), in order to minimize it's inductance and RF resistance. If ribbon is unavailable, then several bonds with round wire should be made to each ground pad. The connection to each DC bias pad per switch, B_1 and B_2, should be made to separated points in the test package, then RF grounded with a high Q (UHF) chip capacitor of at least 100 pF capacity. A typical arrangement is seen in Figure 21b.

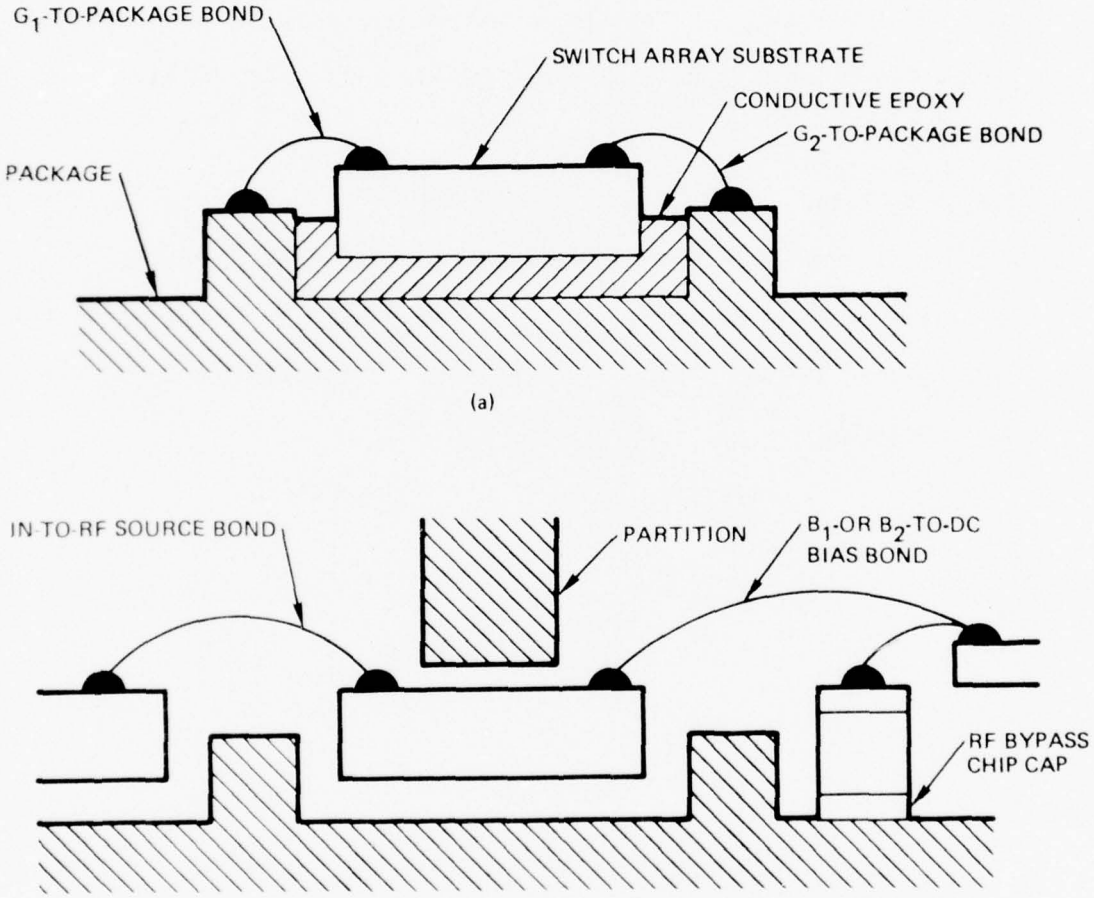


Figure 21. Recommended Package-Chip Configuration

2.6.3 RF Shield

It is recommended that a well-grounded partition be positioned over the switch array as close to the circuit surface as possible as seen in Figure 21b. The shield is necessary to provide some E&M isolation between the input bond wires and the output and DC bias bond wires.

2.6.4 DC Bias

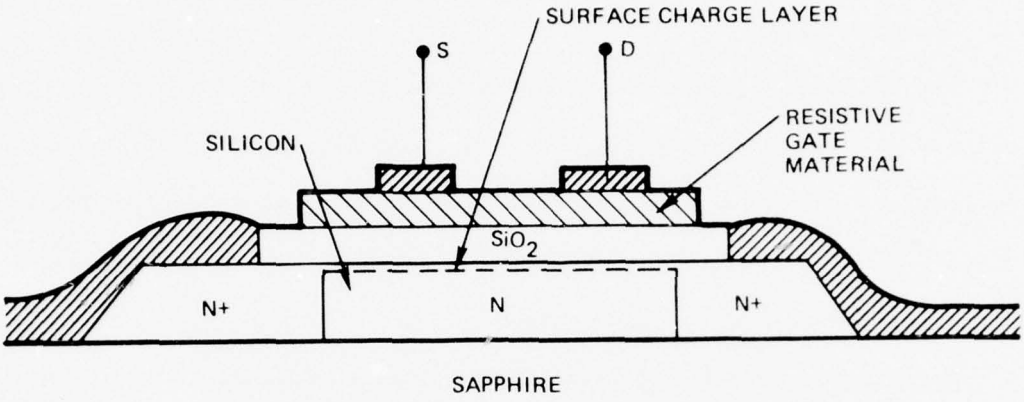
The recommended bias conditions for each switch is +10 mA (2 volts) at bonding pad B_1 and B_2 for ON state and -10 mA (-2 volts) at B_1 and B_2 for OFF state. The absolute maximum current at B_1 and B_2 is $\pm$ 50 mA.

3.0 SILICON-ON-SAPPHIRE RESISTIVE GATE MOSFET SWITCH

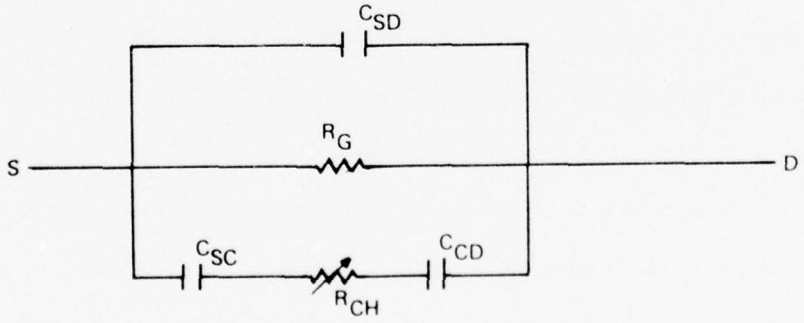
3.1 Introduction

The silicon-on-sapphire Resistive Gate Switch (RGS) is an alternative to the silicon-on-sapphire PIN diode switches developed on this program. The results of an investigation to assess the usefulness of the RGS in the 960-1220 MHz frequency range, and to compare it with the PIN diode switch, are described in this section.

An inherent advantage of the RGS is that it will operate with no DC power drain if it is held in either the ON or OFF condition. The device structure is shown schematically in Figure 22. It consists of a silicon-on-sapphire island with a thermally grown silicon dioxide film on the island. A resistive film on top of the silicon dioxide film has two deposited metal electrodes "S" and "D" which are the input and output RF terminals. The principle of operation is described in terms of the simple equivalent circuit of Figure 22(b). Capacitances C_{SD}, C_{SC}, C_{SD} represent the geometric capacitance between the S and D electrodes, between the S electrode and the Si island, and between the D electrode and the Si island structure, respectively. R_G is the resistance of the resistive film between S and D electrodes, and R_{CH} is the resistance of the N silicon surface channel between S and D. Device geometries and material characteristics are close designed to achieve an acceptable compromise between small C_{SD}, high R_g, and large C_{SC} and C_{CD}. It is then apparent that if R_{CH} can be switched between very high and very low values, an efficient ON/OFF switch will result.



(a) STRUCTURE



(b) EQUIVALENT CIRCUIT

Figure 22. Silicon-On-Sapphire Resistive Gate MOSFET Switch

The switch is turned ON by biasing the resistive gate material positive with respect to the silicon island. This induces a charge accumulation layer on the surface of the silicon island which reduces R_{CH} to a low value, allowing AC current to flow through the switch. Reversing the bias or reducing it to zero eliminates the accumulation layer, R_{CH} reverts back to a high resistance and the switch is turned OFF. The major advantage of this switch over other devices is that no DC power is required to maintain the switch in either ON or OFF positions and only sufficient charge is required during a switching period to accumulate or deplete the surface charge on the silicon island.

Thus, the device will have very low power loss in either ON or OFF state. Various series and parallel combinations can be used to achieve very high ON/OFF ratios in a similar manner to PIN diode configurations but without the DC power requirements. For some applications the switching time required for transition from ON to OFF states and vice versa may be excessive since the surface charging time constant will obviously be a function of the high resistivity of both the resistive film and the silicon-on-sapphire island.

Design of the RGS device essentially reduces to a trade-off between insertion loss, isolation, and switching speed compared to the PIN diode trade-off of insertion loss, isolation, and bias power dissipation. The specifics of the RGS trade-offs are outlined in the following section.

3.2 RGS Equivalent Circuit Model

A comprehensive circuit model used to analyze the RGS switch is shown in Figure 23. The relation of the device structure to the circuit components is as indicated and the following convention is used:

T_1	Resistive Gate Thickness
T_2	Silicon Dioxide Thickness
T_0	Silicon Thickness
R	Resistivity of Gate Material (ohm cm)
R_0	Resistivity of Silicon-On-Sapphire (ohm cm)
L	Separation Between Contacts on Resistive Materials - Also Contact Width Since 1:1 Width / Space is Used
W	Width of Resistive Material in Direction Perpendicular to Plane of Figure 23
ε	Permittivity of Silicon Dioxide.
R_1	Radiation Resistance of Transducer Source
C_1	Capacitance of Transducer Source
μ	Electron Mobility in Silicon-On-Sapphire

The value of R_7, assuming ohmic contacts between metal and resistance gate material and $L >> T_1$ (both valid assumption), is given by

$$R_7 = \frac{RL}{wT_1}$$

Resistance R_{10} is a function of the bias across the resistive gate/silicon dioxide combination. A negative bias of V volts on the silicon induces a surface accumulation layer which results in a value of R_{10} given by

$$R_{10}\ (ON) \approx \frac{T_2 L}{\varepsilon \mu W V}$$

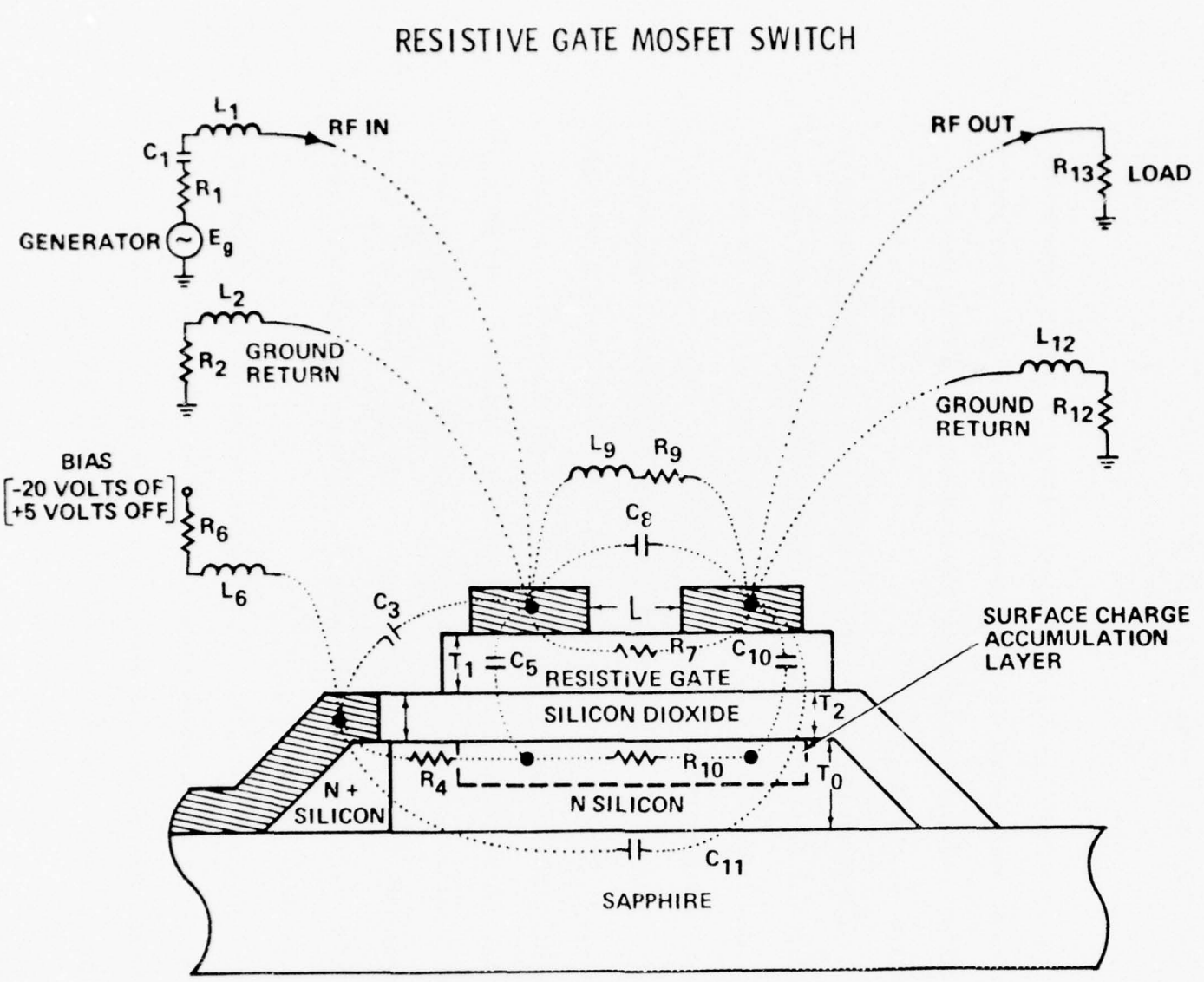


Figure 23. Resistive Gate MOSFET Switch

A positive bias applied to the silicon gives

$$R_{10}\ (OFF) \simeq R_0 \frac{2L}{WT_0}$$

Capacitances C_3, C_8, and C_{11} are coplanar geometric capacitances due to adjacent metal stripes on the surface and can be calculated by conformal mapping techniques as described in the previous report, AFGL-TR-76-0016, (pg. 19).

Capacitances C_5 and C_{10} are parallel plate capacitances of values readily calculable from the metal stripe area and dielectric thicknesses.

The value of R_4 is due to silicon resistance and for the geometry shown is approximately equal to $R_{10}(OFF)$.

Inductors L_2, L_6, L_{12} and their associated series resistances R_2, R_6, R_{12} are isolating inductors to allow charging and discharging the accumulation layer while presenting a high impedance to ground at 1 GHz. Either L_2 or L_{12} could be eliminated without significantly affecting device performance. Provision is made in the circuit model to parallel tune C_8 with L_9 to improve isolation. Inductor L_1 is used to series tune the transducer source capacitance C_1 at center frequency to reduce insertion loss.

For compact integrated switch arrays comparable to the PIN versions described in the previous section, it will be necessary to integrate the inductors on the same sapphire substrate as the RGS. An acceptable device geometry must therefore be selected which is compatible with feasible thin film spiral inductor values.

The single device circuit model of Figure 23 was analyzed while holding the following parameters constant. The constant values were

R_1 = 20 ohms

C_1 = 2 pf

$R_2=R_6=R_{12}$ = 50 ohms

$L_2=L_6=L_{12}$ = 50 nh

R_{13} = 50 ohms

$T_1=T_2$ = 1000 angstroms

Parameters varied to assess the effect of device geometry and material properties on switch performance were W, R, and R_0. The parametric search was made both with and without the parallel tuning inductor L_9. The results of this evaluation are summarized in Figures 24 to 26.

Figure 24 shows the performance of an RGS as a function of silicon resistivity from 2 ohm cm to 92 ohm cm.

The dotted line is the performance of a typical single series connected PIN switch (forward resistance ~20 ohms, reverse capacitance = .1 pf for comparison. Also included is the isolation predicted if the parallel tuning inductor L_9 is omitted, in this case the curves for R_0 = 12, 22, 52, 92 all collapse onto the 12 dB curve joining the triangular plot points. For this figure R = 1100 ohm cm, w = .6 cms, and L_9 is 43 nH. The switching time for this device is ~5 μsec, primarily determined by the high gate resistivity. Figure 25 repeats Figure 24 with w = .2 cms which changed L_9 to 129 nH. As can be seen the isolation improved by ~10 dB at the expense of ~3 dB extra insertion loss.

Variation of RGS performance with gate resistivity is shown in Figure 26 for R_0 = 92 ohm cm, w = .6μ, and L_9 = 43 nh. The difference in ON/OFF ratio for 100 vs 1100 ohm cm is seen to be small although the switching times were .52μsec vs. 5.7μsec respectively.

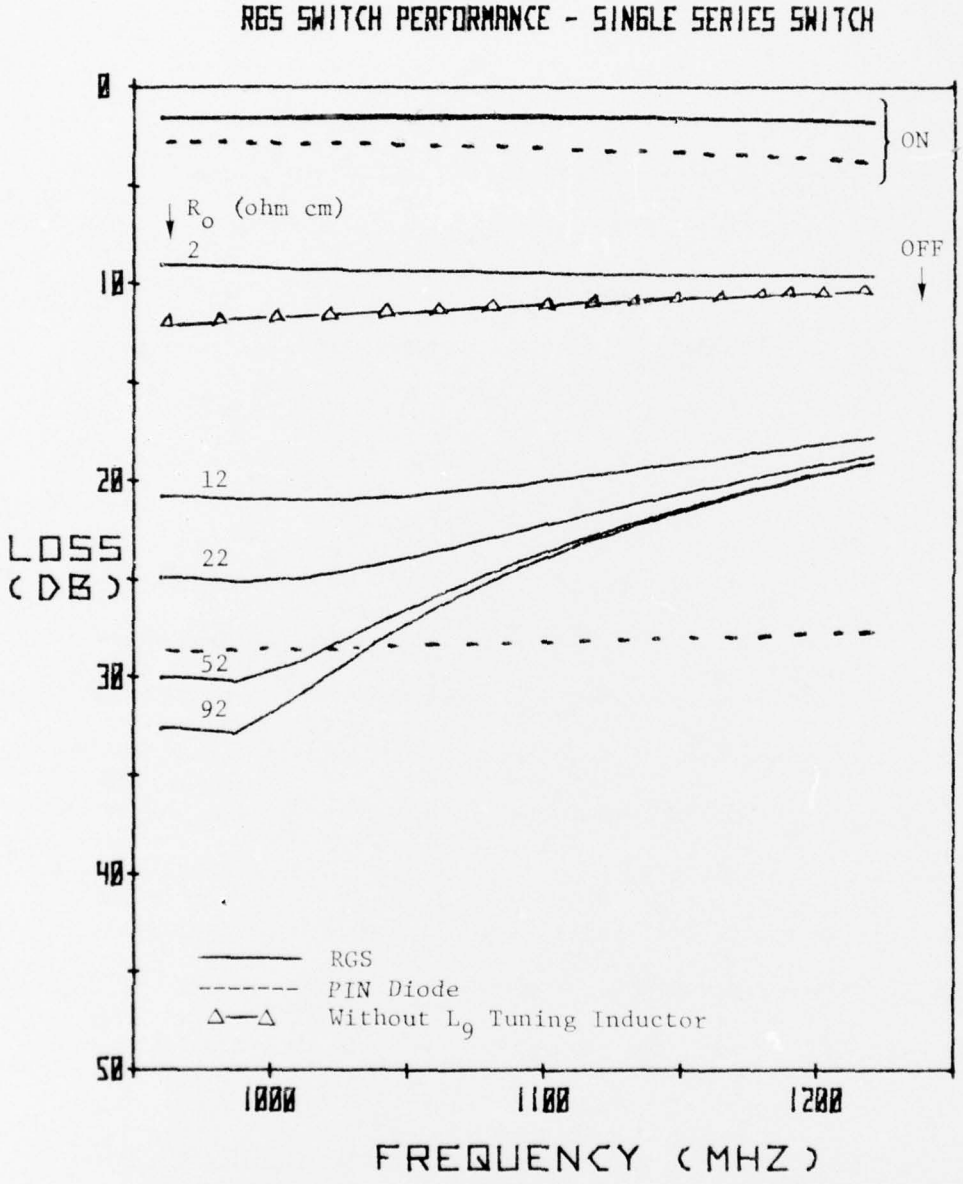


Figure 24. RGS Performance Vs. Silicon Resistivity (W = 0.6 cm)

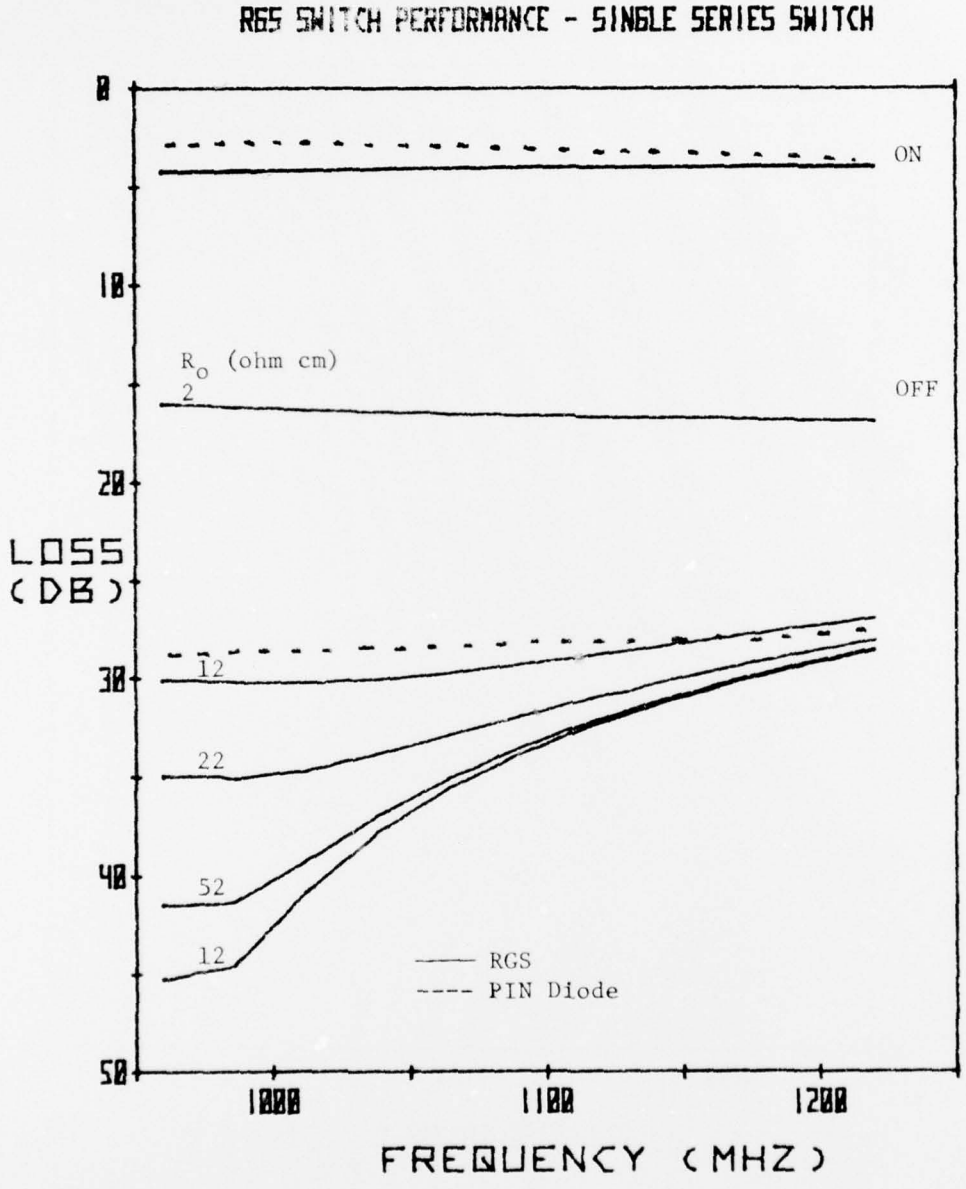


Figure 25. RGS Performance Vs. Silicon Resistivity (W = 0.2 cm)

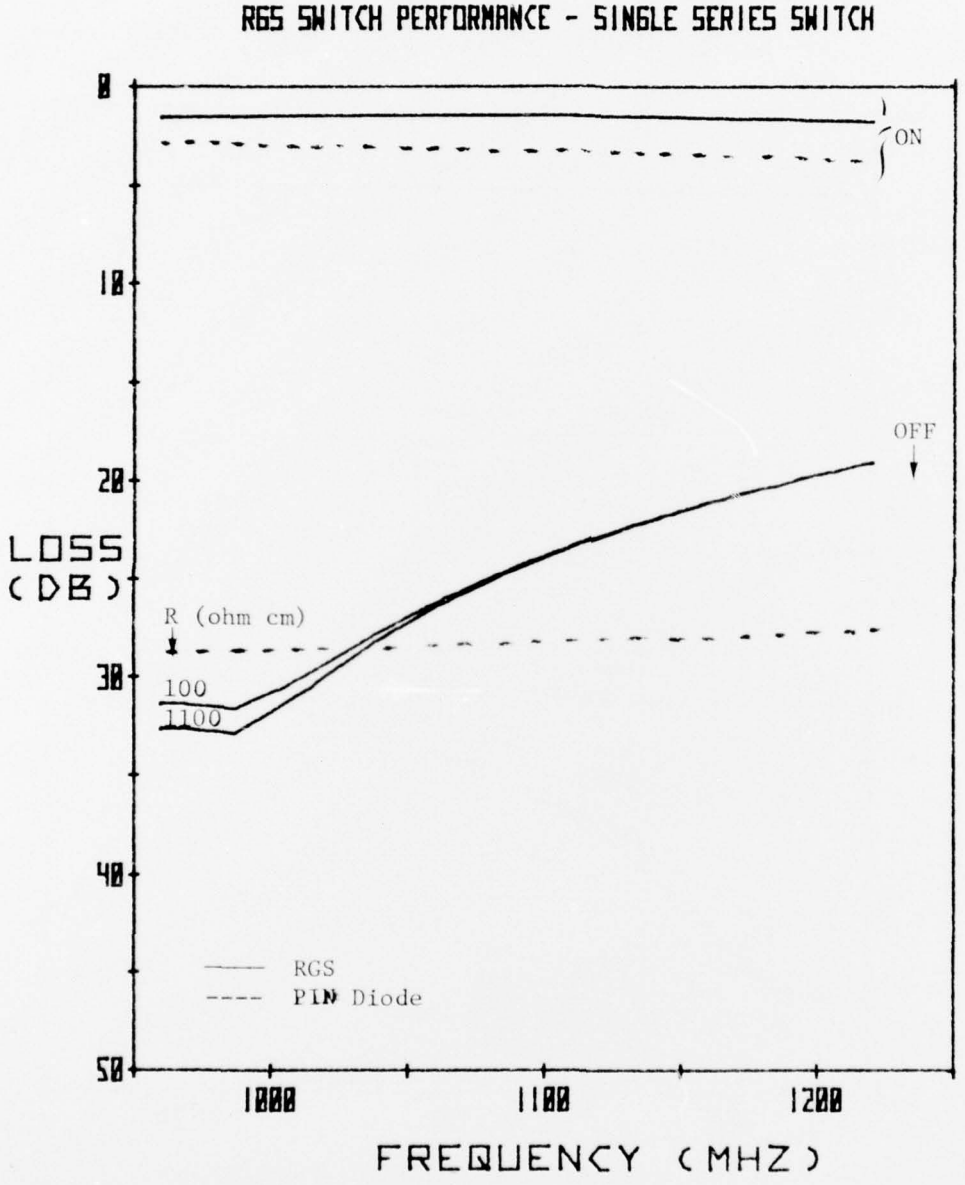


Figure 26. RGS Performance Vs. Gate Resistivity

3.3 Experimental Results

The dimensions of the initial RGS design are: L = 8 μm, $T_1 = T_2 = 0.1$ μm, and W = 4000 μm. The resistive gate material is RF sputtered titanium dioxide (TiO_2). It was found that the TiO_2 chemical etch rate was very low. Consequently, the gate pattern of TiO_2 was defined by RF sputtering etching using SiO_2 as a mask. The RF performance of an RGS device is seen in Figure 27, which shows the insertion loss of the device for various bias voltages in the frequency range 0.1 to 1.1 GHz. The on/off ratio varies from 24dB to 8.5dB. The resonance at 0.18 GHz is due to the RF choking inductor used in the test fixture, and indicates that the true insertion loss of the switch at zero bias is probably higher. Thus, the true on/off ratio is also higher. The large DC voltage required to turn on the switch is believed due to charge fixed at the material interfaces. This residual charge can probably be removed by annealing and reduction of the dielectric film thicknesses.

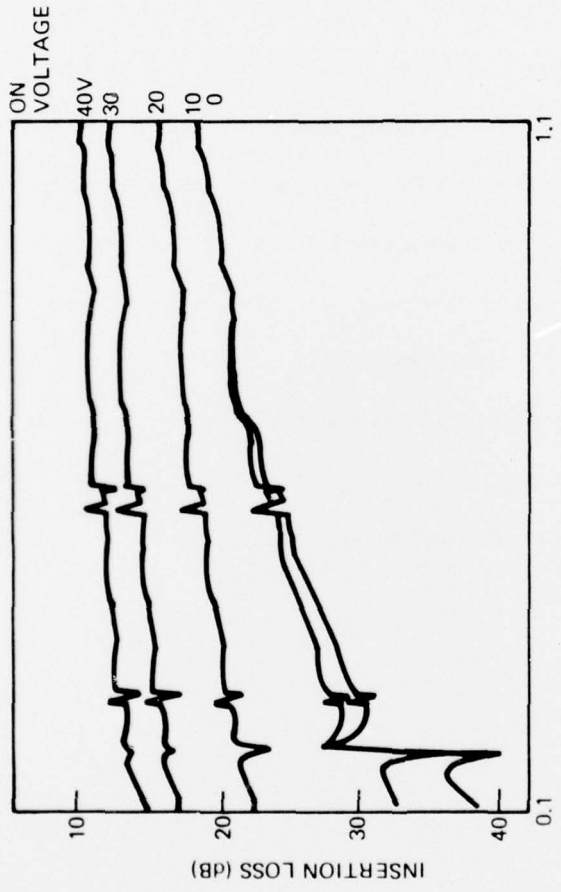


Figure 27. Experimental Performance of RGS

4.0 SILICON-ON-SAPPHIRE 1 GHz MOSFET

The major effort on this program has been to develop the integrated silicon-on-sapphire PIN diode switching array/multiplexer for use in the output stage of a frequency synthesizer which uses a surface acoustic wave filter bank. Due to the insertion losses of the SAW filters and the multiplexer, the output signal will probably require amplification prior to being used as a carrier or modulating signal. Accordingly, a minor task was included in this program to assess the feasibility of integrating amplifiers on the same sapphire substrate as the PIN diode switch array.

A silicon-on-sapphire MOSFET device was included in the final PIN diode switch photomasks. By the addition of one extra mask layer and one extra processing step, this MOSFET was fabricated using the same processing sequence as the PIN diode switch array. The MOSFET structure is an N^+NN^+ structure with a 3 micron source to drain spacing and 4,000 micron gate width. A gate oxide thickness of 1,000Å then gave a transductance in the 15-20 mmhos range. The device was evaluated over the .7 GHz-1.5 GHz frequency range, and the S parameters obtained in a 50 ohm system are shown in Figure 28. The maximum available gain calculated from the S parameters is shown in Figure 29 to be >10dB up to 1.5 GHz.

This data demonstrates feasibility for integrating the MOSFET devices on the same sapphire substrate as the PIN diode switches. Addition of suitable biasing and isolation elements such as resistors, DC-blocking capacitors, etc., similar to those used in two

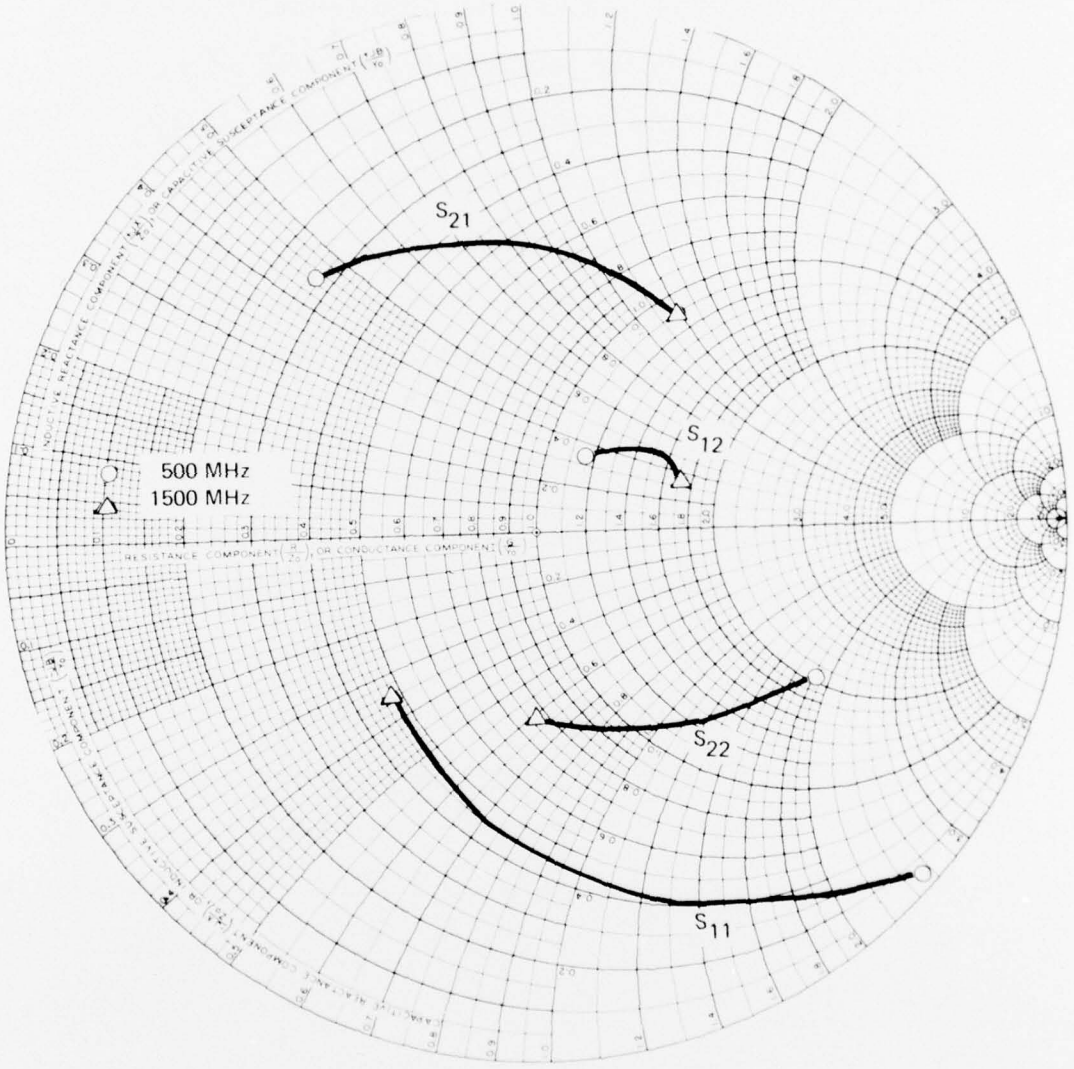


Figure 28. Silicon-On-Sapphire MOSFET S Parameters

Radius for S_{11}, S_{12}, S_{22} = 1,

Radius for S_{21} = 2.5

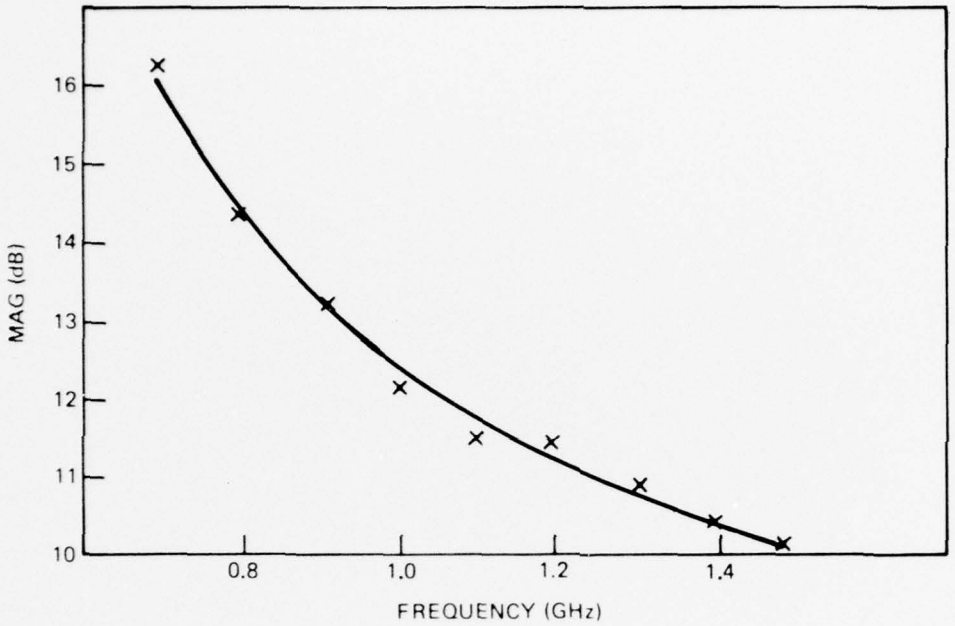


Figure 29. Silicon-On-Sapphire MOSFET Performance

(Maximum Available Gain Vs Frequency)

versions of the PIN diode multiplexers, should allow the fabrication of integrated multi-stage monolithic amplifiers.

5.0 CONCLUSIONS AND RECOMMENDATIONS

The feasibility of a compact, monolithic, 16-input, 1-output UHF switch using SOS technology was demonstrated. A comparison of actual performance with performance goals is seen in Table 5.

1. The measured on/off ratio varied from 57.5dB to 62dB. The true on/off ratio of the switch is probably higher although it is extremely difficult to reduce stray RF feed-through.

2. By developing the technology for integrated RF chokes, the DC power requirements per switch have been reduced from 50mW of the previous device, to 30mW. The use of integrated inductors has also eliminated the less reliable MOS capacitors which were used for DC blocking in the previous switch array.

3. A limited theoretical and experimental investigation of a Resistive Gate Switch (RGS), has yielded very encouraging results. An analysis of the device was presented which predicts that the RGS should have as high on/off ratio as an SOS PIN diode yet dissipate no static power. The initial experimental results indicate that a multi-RGS switch is feasible.

4. An SOS MOSFET with good performance up to 1.5 GHz has been demonstrated. The maximum available gain per FET is 10dB at 1.5 GHz in a structure which is physically compatible with the present switch arrays. Thus, the development of an integrated amplifier array to be used in conjunction with a UHF switch array appears quite feasible.

Table 5 Comparison of Actual Performance With Performance Goals

ITEM	GOAL	ACHIEVED
Frequency of Operation	950-1220 MHz	950-1220 MHz
On/Off Ratio	65dB	57.5-62dB
DC Power Dissipation	$\leq$ 40mW/Switch	20-30mW
Insertion Loss Uniformity	1dB	1.5dB
Switching Time	$\leq$ 1 µsec	$\leq$ 2 nsec
Power Handling Capability	$\geq$ 10mW	15mW

The integrated RF inductor technology makes it possible to develop a high on/off ratio switch array using the RGS approach. The zero state power dissipation makes these devices very desireable in systems where low DC power dissipation is important. Further work is recommended to optimize the RGS and develop an RGS switch array. Further work is also recommended to develop an FET amplifier array to be used with the UHF switches.

METRIC SYSTEM

BASE UNITS:

Quantity	Unit	SI Symbol	Formula
length	metre	m	...
mass	kilogram	kg	...
time	second	s	...
electric current	ampere	A	...
thermodynamic temperature	kelvin	K	...
amount of substance	mole	mol	...
luminous intensity	candela	cd	...

SUPPLEMENTARY UNITS:

plane angle	radian	rad	...
solid angle	steradian	sr	...

DERIVED UNITS:

Acceleration	metre per second squared	...	m/s
activity (of a radioactive source)	disintegration per second	...	(disintegration)/s
angular acceleration	radian per second squared	...	rad/s
angular velocity	radian per second	...	rad/s
area	square metre	...	m
density	kilogram per cubic metre	...	kg/m
electric capacitance	farad	F	A·s/V
electrical conductance	siemens	S	A/V
electric field strength	volt per metre	...	V/m
electric inductance	henry	H	V·s/A
electric potential difference	volt	V	W/A
electric resistance	ohm		V/A
electromotive force	volt	V	W/A
energy	joule	J	N·m
entropy	joule per kelvin	...	J/K
force	newton	N	kg·m/s
frequency	hertz	Hz	(cycle)/s
illuminance	lux	lx	lm/m
luminance	candela per square metre	...	cd/m
luminous flux	lumen	lm	cd·sr
magnetic field strength	ampere per metre	...	A/m
magnetic flux	weber	Wb	V·s
magnetic flux density	tesla	T	Wb/m
magnetomotive force	ampere	A	...
power	watt	W	J/s
pressure	pascal	Pa	N/m
quantity of electricity	coulomb	C	A·s
quantity of heat	joule	J	N·m
radiant intensity	watt per steradian	...	W/sr
specific heat	joule per kilogram-kelvin	...	J/kg·K
stress	pascal	Pa	N/m
thermal conductivity	watt per metre-kelvin	...	W/m·K
velocity	metre per second	...	m/s
viscosity, dynamic	pascal-second	...	Pa·s
viscosity, kinematic	square metre per second	...	m/s
voltage	volt	V	W/A
volume	cubic metre	...	m
wavenumber	reciprocal metre	...	(wave)/m
work	joule	J	N·m

SI PREFIXES:

Multiplication Factors	Prefix	SI Symbol
1 000 000 000 000 = 10^{12}	tera	T
1 000 000 000 = 10^{9}	giga	G
1 000 000 = 10^{6}	mega	M
1 000 = 10^{3}	kilo	k
100 = 10^{2}	hecto*	h
10 = 10^{1}	deka*	da
0.1 = 10^{-1}	deci*	d
0.01 = 10^{-2}	centi*	c
0.001 = 10^{-3}	milli	m
0.000 001 = 10^{-6}	micro	μ
0.000 000 001 = 10^{-9}	nano	n
0.000 000 000 001 = 10^{-12}	pico	p
0.000 000 000 000 001 = 10^{-15}	femto	f
0.000 000 000 000 000 001 = 10^{-18}	atto	a

* To be avoided where possible.

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